Update on the status LHC interlocked BPMs at Pt6

- Introduction to the HW layout
- Status of the MPP actions list during the last meeting
- FE HW intensity dependence transfer function
- System issues in high sensitivity mode
- Strategies to solve them
- Interlock test & debugging system in Pt6
- Introduction to the current interlock process logic
- New features in development and test
- Ideas about future upgrades

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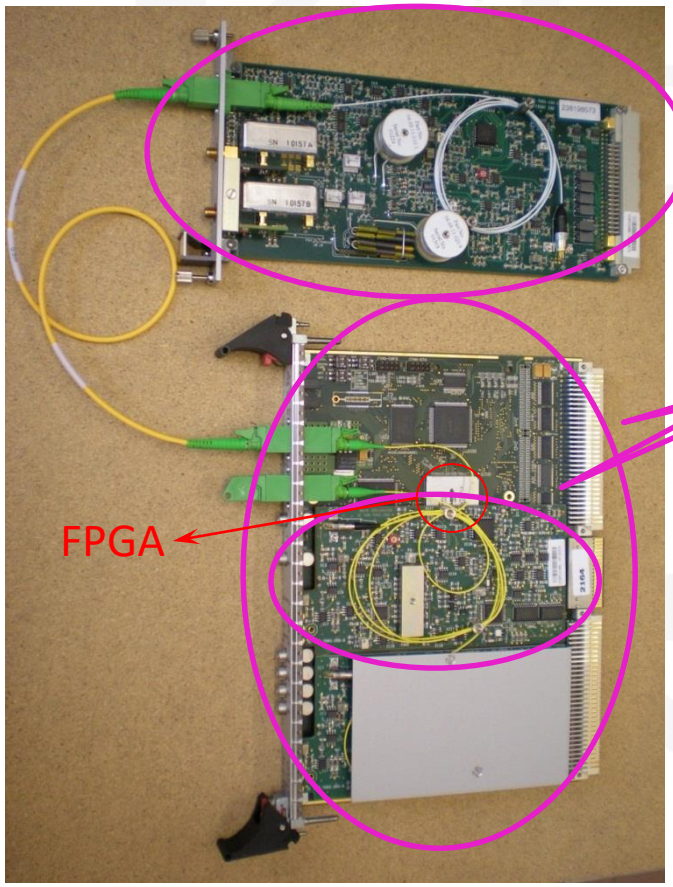
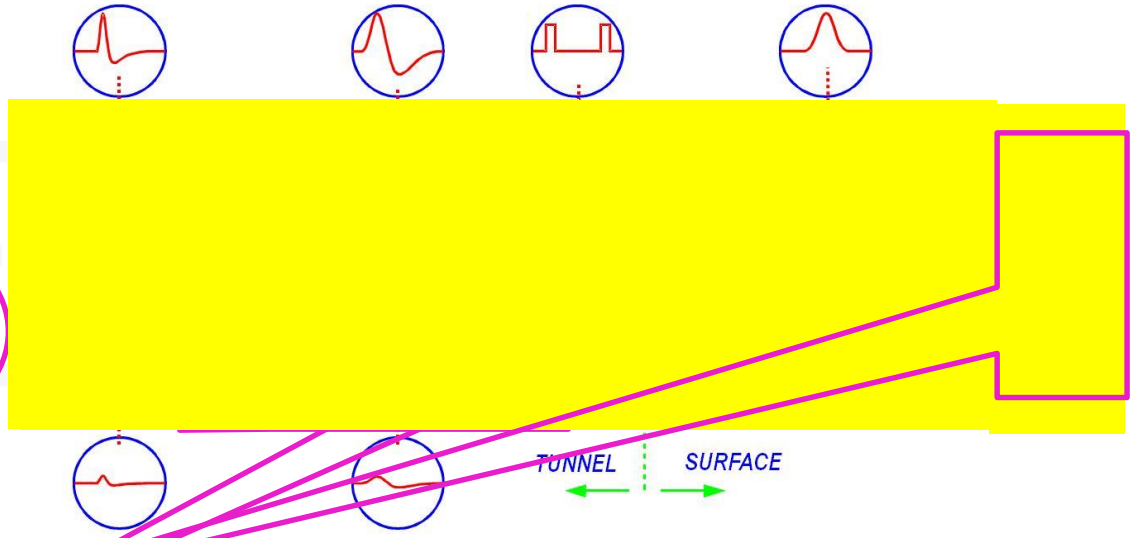
Introduction - Layout





- The electronics consist on the standard LHC BPM front-ends, BUT with an additional process running in FPGA firmware in the Digital Acquisition Board.
- Parallel processes at the DAB FPGA : Async. and Sync. Orbit, the Post-Mortem, the Capture and the interlock!
- The mezzanine provides to the DAB 1 asynchronous ADC sample per bunch.

MPP meeting action list for Pt6 BPMs

① Replace the attenuators during TS2 in order to align the low sensitivity limit of all the Pt6 BPMS interlocked channels at 2e10 p^+/bunch.

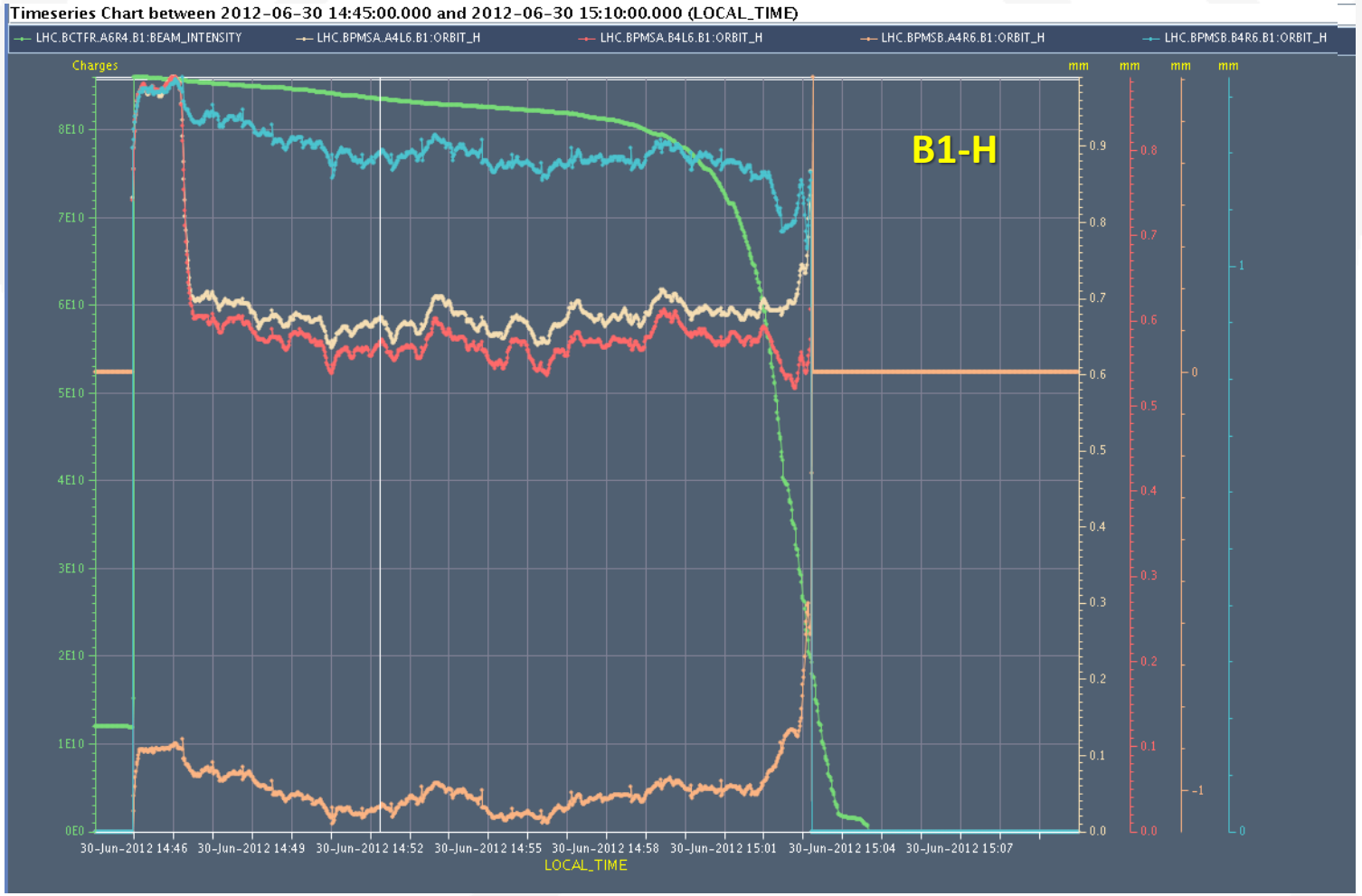
② Verify that the sensitivity limits are correct after the change. And that the position interlock thresholds are still valid.

③ Install a test & debugging BPM interlock system in Pt6 and deploy the new FESA and firmware versions on it.

④ Test with beam the new proposed features before deploy them into the operative system. Report the test results to the MPP WG.

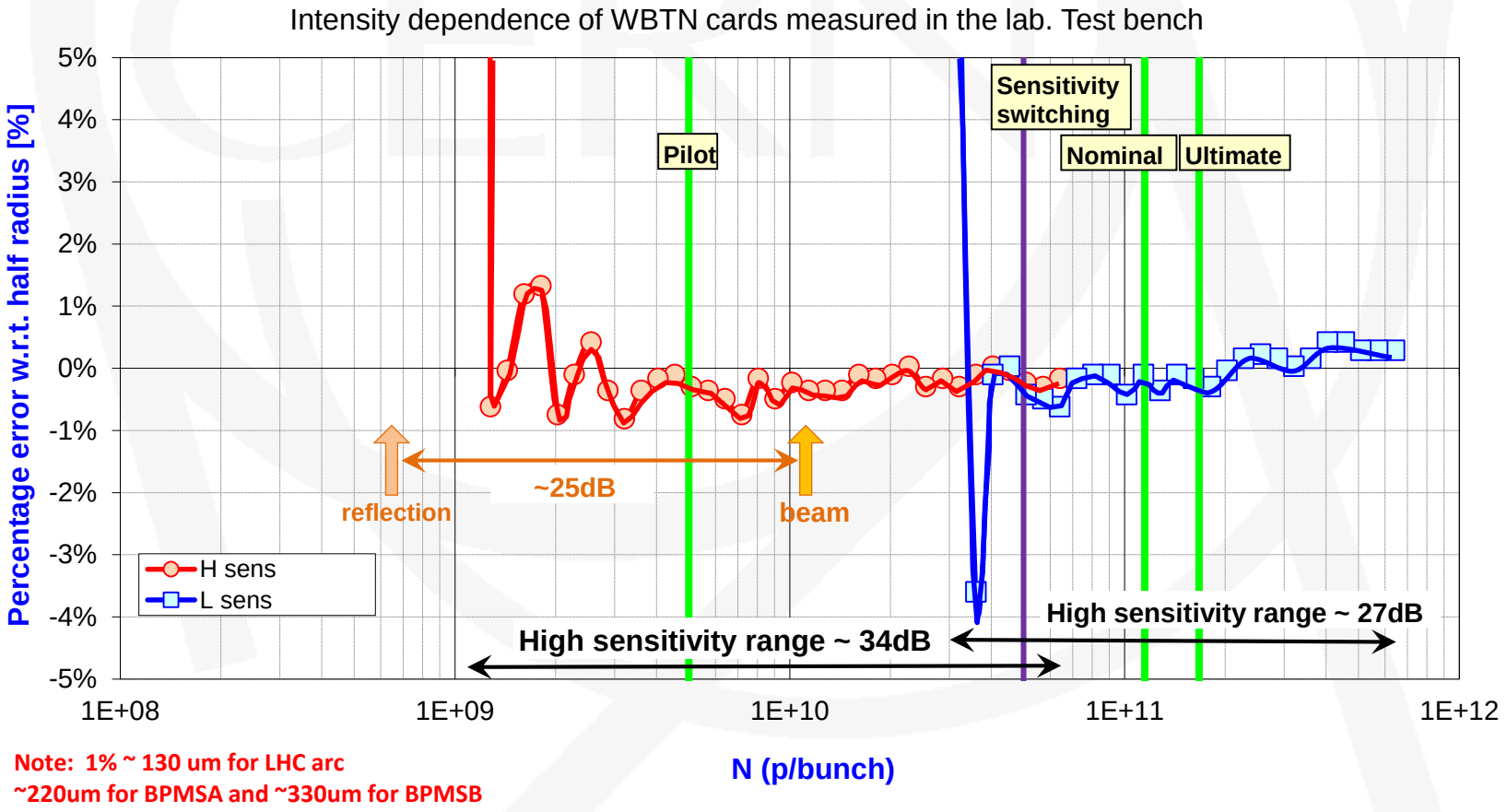
1) Attenuator change

- **Scrapping performed on 29/6/2012 in low sensitivity range.**



WBTN intensity dependence

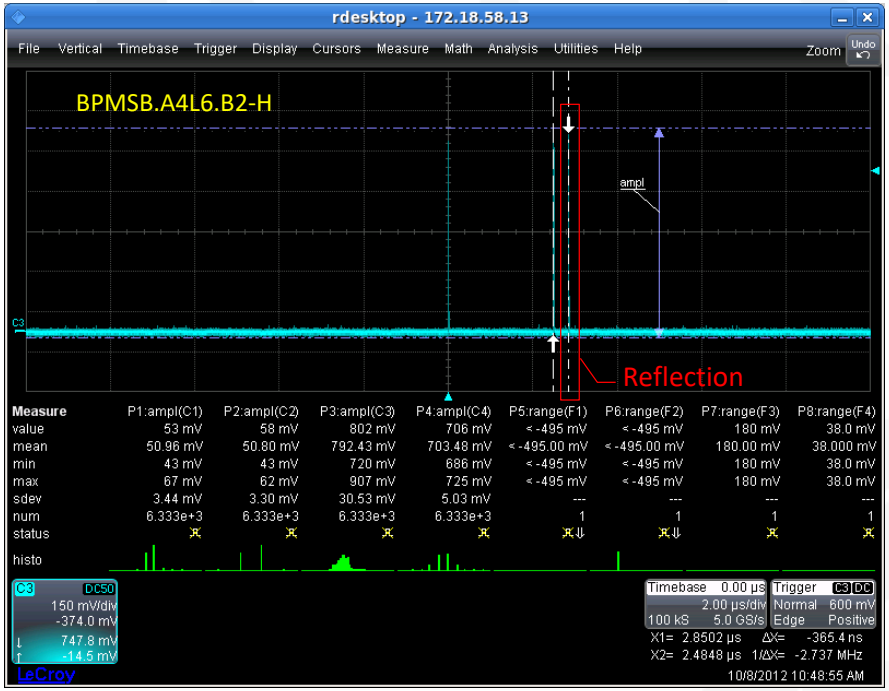
- **Current installation BPMSA (80mm ap.) have 4dB and BPMSB (130mm ap.) have 0 dB.**
- **Unfortunately during the proton-ion MD (~6e9p/b in B2, and ~1.3e10 p/b in B1) the proton beam was dumped several times.**
  - Hypothesis was that while this setup works reliably when BPM are working in low sensitivity range, it makes the system too vulnerable to reflections when working in high sensitivity.

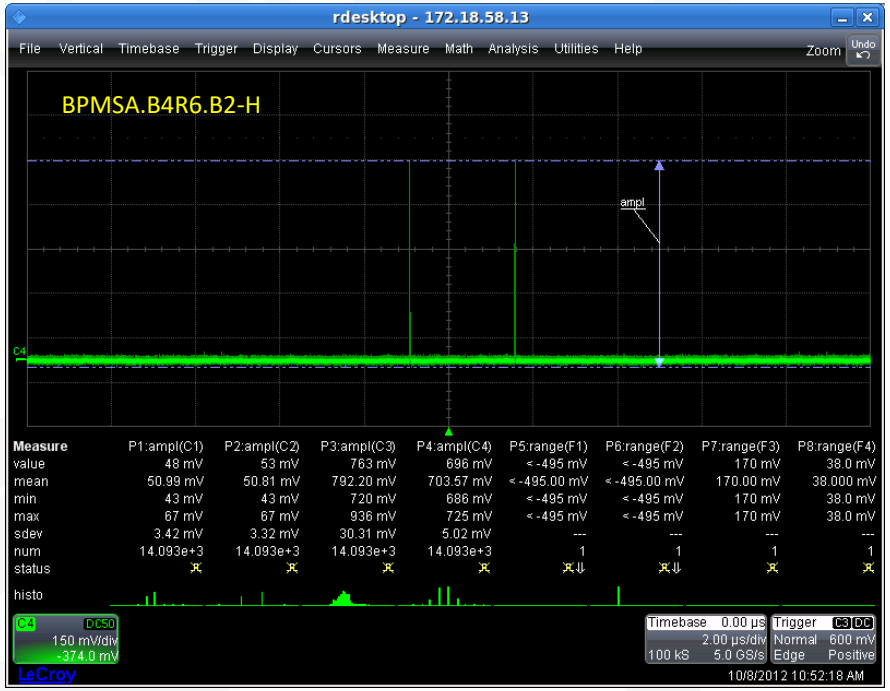


Note: 1% ~ 130 um for LHC arc
~220um for BPMSA and ~330um for BPMSB

8th October BI-BPM MD

- During BI MD on 8 Oct. two bunches were injected on B2 : 9e9p (bk 1) and 3.06e10p (bk 1001). (Unfortunately B1 was not available.)
- Reflections were confirmed in the two BPMSB type monitors of B2, but not seen in the BPMSA type. They started disappear when the fat pilot was scrapped to ~1.5e10p.
- However, during the MD proton-ion (on 14 Sept.) BPMSA.A4L6.B1-V showed additional triggers with probes above 1e10p/b.



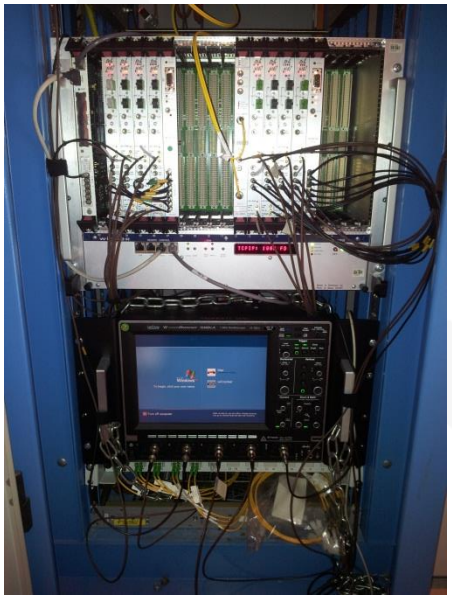


Conclusions of intensity dependence

- **In high sensitivity mode the interlocked BPMs are sensitive enough to detect reflections and trigger the interlock on them.**
- **Different strategies of combating this:**
  - As immediate solution, attenuators can be replaced once more before the proton-ion run, but this will not be a permanent solution.
  - We can try to adjust the low and high dynamic ranges of the interlocked cards differently, however this does not seem a long term solution neither, since beams with 4-5e10p/bunch, will still create reflections with amplitudes similar to those BPM signals produced by beams >2e9p/bunch.
  - Another solution would be to place remotely controllable variable attenuators.
  - The card has a simple circuit that once the bunch signal has passed, any signal arriving a few ns later can be blocked. Adjusting the cable length we can try that the reflections arrive during this "blocked" periods.
  - Another possibility would be to install absorptive filters close to the monitor.
- **We should try to reproduce the effect during a TS with a generator in order to find the exact location of the defect that creates the reflection, and try different techniques to remove it or mitigate it. In any case, further studies and measurements are necessary (access UA63 an UA67).**

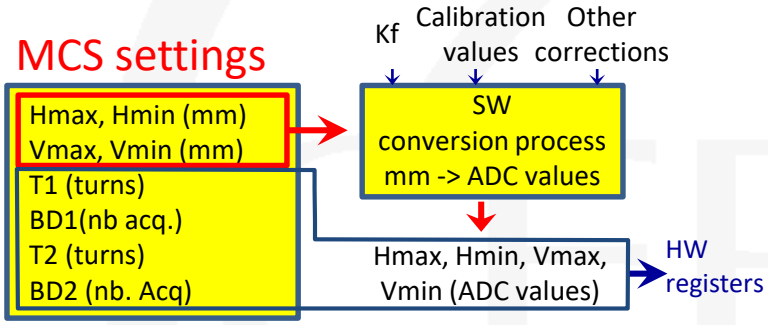
2) Test and debugging system

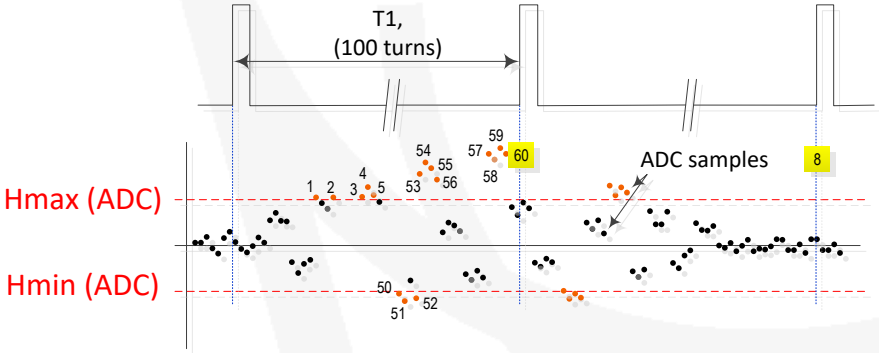
- **Most of the issues have been originated at the analogue electronics part, and not at the digital acquisition HW or at the software level. However, firmware and software are the tools available to diagnose why a beam was dumped.**
- **In a few occasions, the beam was dumped and the operator does not know why it happen. So several firmware and software proposals are in development to improve this situation.**
- **In order to test them without impact for the LHC operation, a test system has been installed in Pt6.**



- Operational system: The signals arrive to the operational BPM interlocked crates (bpmint1 and bpmint2) from the FE cards located in UA67 &UA63 through optical fibers.
- Test system: All the digital acquisition part has been duplicated. It consist on a VME crate and CPU (bpmint3) + 8 DABs.
- Operational DABs in bpmint1 and 2 act as signal repeaters, feeding the cards in bpmint 3 with real beam data.
- DAB cards are identical, but FPGA firmware and FESA software have new features.
- Test DABs cards act also as repeaters that feed a remotely accesible oscilloscope.

Introduction – Interlock process





As described in the LHC beam dumping system Technical Specification (EDMS link), these are the MCS-managed parameters to decide whether to trigger the beam dump:

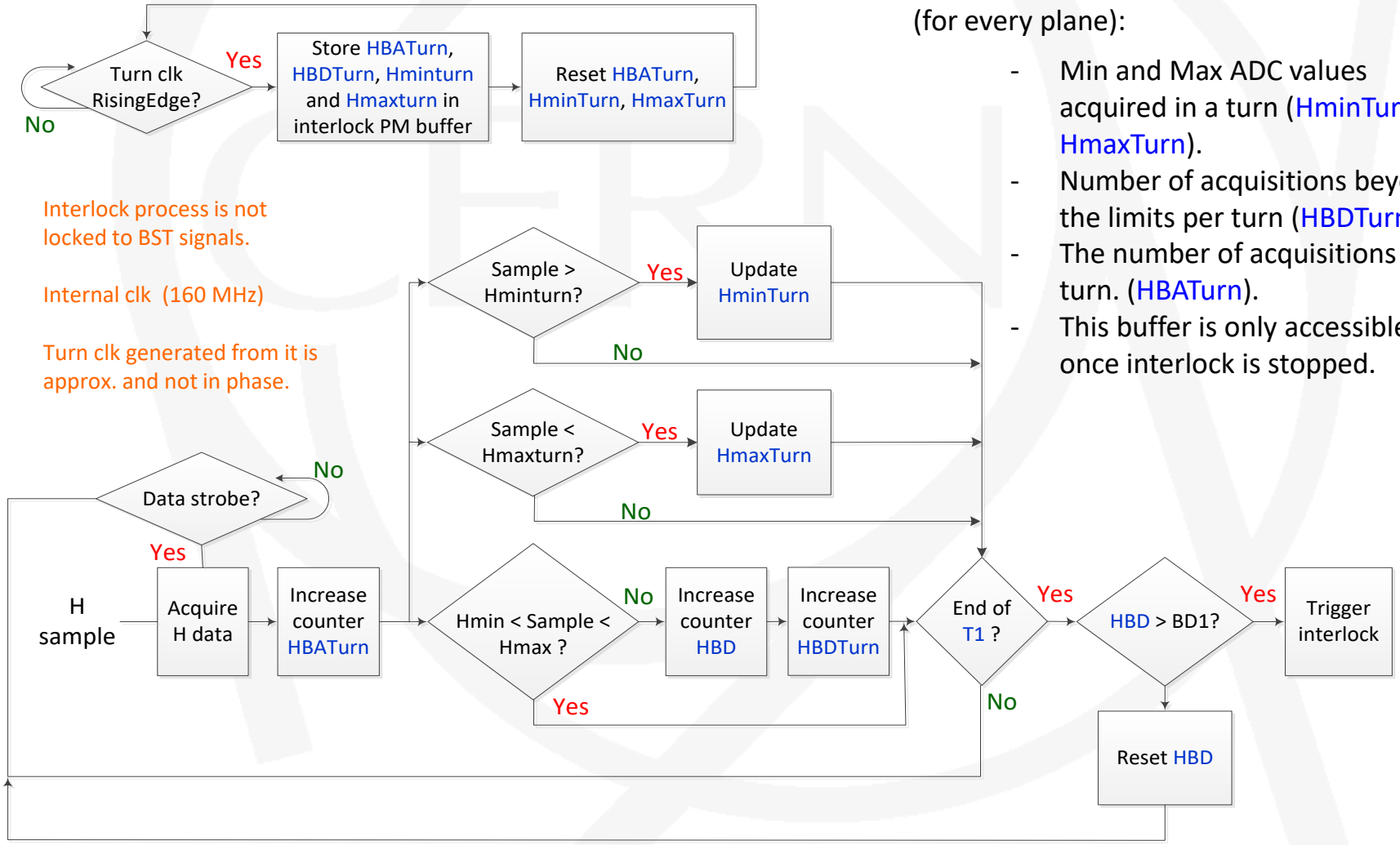
1. Hmax , Hmin, Vmax and –Vmin: actual position thresholds (nominally 3.5 mm). These will be entered into the FPGA by the FESA front-end as four 10-bit numbers corresponding to these limits after taking into account the calibration factors for the BPM and electronics.

2. T_1 and T_2 which define the length of the time windows expressed in number of turns.

3. BD_1 and BD_2 which define the maximum number of bunches which may be outside the position threshold defined in 1) within the corresponding time window defined in 2) before a dump is triggered.

- Currently 70 readings (BD1) out of limits over 100 turns (T1) triggers the system (i.e. <1 bunch/turn)
- Second window with 250 (BD2) out of limits over 10 turns (T2) to quickly catch fast orbit change.
- Errors currently counted as “out of allowed window”.
- It’s typically on errors that we trigger the system when bunch intensity drops to threshold levels

Introduction – Interlock process



The interlock Post-Mortem buffer contains (for every plane):

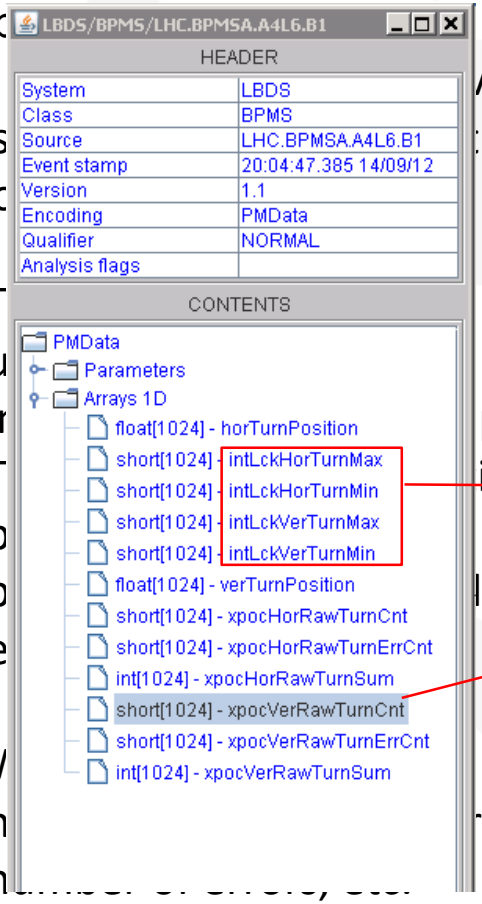
- Min and Max ADC values acquired in a turn (HminTurn, HmaxTurn).
- Number of acquisitions beyond the limits per turn (HBDTurn).
- The number of acquisitions per turn. (HBATurn).
- This buffer is only accessible once interlock is stopped.

New firmware and FESA changes

- **New settings to define the max. number of wrong acquisitions during T1 and T2: HErrorT1, HErrorT2, VErrorT1 and VErrorT2.**
  - HBD counts only the correctly acquired bunches whose positions are effectively beyond the limits. Errors are counted separately.
  - This would allow to relax the settings in order not to dump the beam when a single bunch is acquired incorrectly (bunch charge close to the limits of the dynamic range).
- **Additional registers to know in "real time" the interlock behaviour: Number of bunches outside limits and number of errors during last T1 and T2 period.**
  - This allows some diagnostics of what is happening before the beam is effectively dumped.
- **Additional Post-mortem fields: Number of errors per turn and turn flags to indicate the start of T1 and T2 periods.**
  - This allows to reconstruct exactly the history of the interlock process.
- **When 1 card triggers a dump, now we can "freeze" the post-mortem buffers of the rest cards.**
  - Post-Mortem analysis was complicated because the buffers of the cards that did not trigger were overwritten, and data among channels was not aligned in time.
- **Hmax, Hmin, Vmax and Vmin will now be persistent fields. Before they were calculated at every reboot of the Front End taking the last calibration values at that time (not always 50ns filling pattern).**
- **Hmax, Hmin, Vmax and Vmin were calculated without taking into account the non-linearity of the WBTN cards. The interlock effective margin was smaller than initially defined. Machine was more safe, but availability was smaller.**

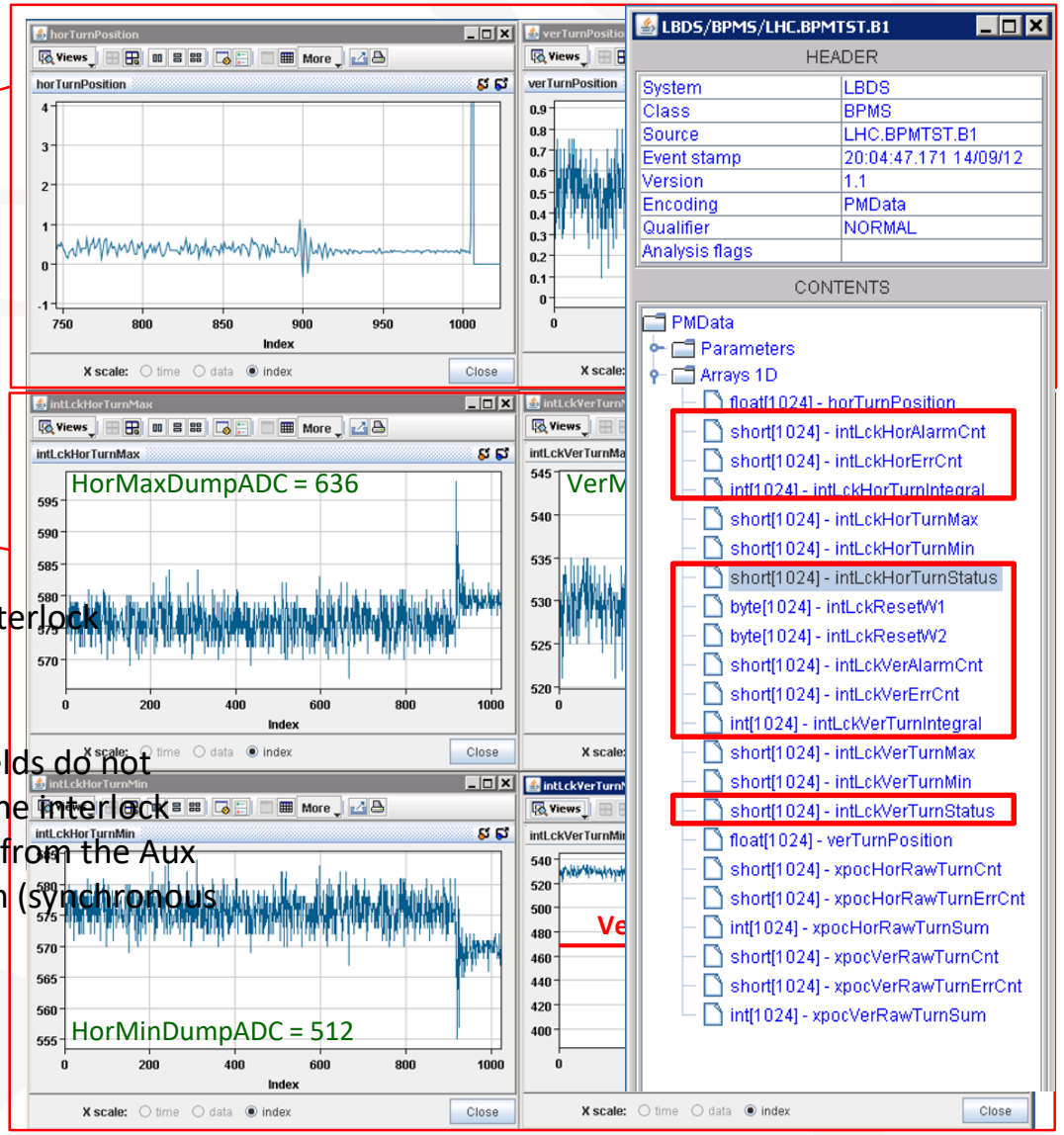
Post-mortem buffers

Horizontal and vertical trajectories and the average of all the valid



Data from interlock process

The other fields do not come from the interlock process, but from the Aux Post-Mortem (synchronous process).



Post-Mortem Analysis tool

- **However, these seems still expert tools. They requires a bit of data mining…**
- **I believe that this reveals the necessity of improving the diagnostics tools with a layer above FESA and/or the PM Data Viewer.**
- **Requirements/Proposals:**
  - Add to the logbook message the channel that triggered first, and not only the crate. (“Syst. A”/”Syst.B”).
  - Create a Expert GUI, with the Hmin/Hmax/Vmin/Vmax data turn by turn and the limits.
  - Additionally, show the errors and the number of acquisitions per turn.

Conclusions and future steps

Experience with the new system:

Unfortunately, the new firmware and FESA are not yet ready for deployment. A few small issues affecting the logged data in the Post-Mortem should still be solved and tested.

Future steps (LS1):

- **Investigations ongoing to try and address remaining shortcomings of current system:**
  - Extend the dynamic range of the two working modes (high and low sensitivity) without compromising the reliability and the availability.
  - Provide bunch-by-bunch post-mortem buffers (?)
- **In order to increase the memory available an increase the bunch by bunch post-mortem data, the number of DAB cards for these monitors can be duplicated, and the signals split in surface. This way, half of the cards will be dedicated only to the interlock process, while the rest will take care of the orbit and capture modes.**
- **The FPGA present in the PT6 BPMS DAB cards can be upgraded to a bigger IC.**
- **The detection threshold of the low sensitivity range should be made still longer, with a lower limit of about 1e10p/bunch at 7TeV. This will make the system again sensitive to the reflections, this time also in the low sensitivity range. So, the reflection source should be found and mitigated.**
- **A software additional layer that makes easier and faster analysing the interlock PM buffers should be put in placed.**

Thank you

Spares