

Powering interlock changes during LS1

I. Romera
on behalf of TE-MPE-MS...

Outlook

- **Powering Permit 60A**
- **Access powering interlocks**
- **Global protection mechanisms**
- **Other activities**

Beam dump after losing PP_60A

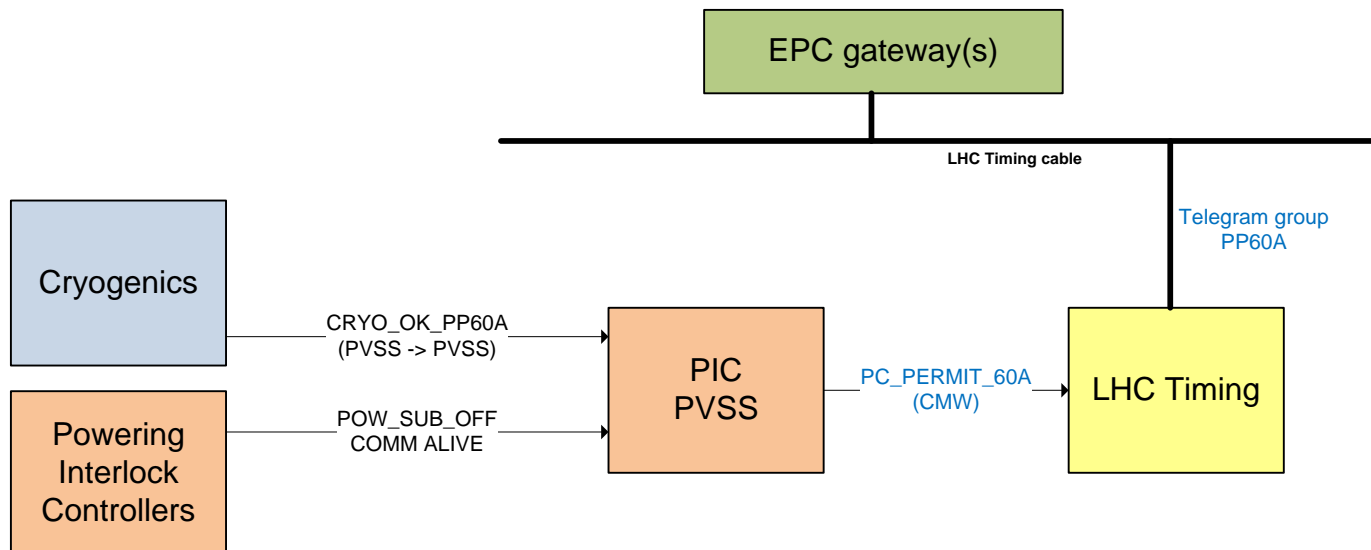
- 25.Oct.2012 16:23:18.685 => Beam dump at stable beams
 - Reason: Orbit correctors switched off before the dump

The screenshot displays the 'bic_eventseq' software interface. The title bar indicates 'Version: 0.4.11' and 'Responsible: Ivan Romera Romerez'. The interface is divided into several sections:

- HEADER:** Contains system information such as System (BIC), Class (EVENT_SEQ), Source (ISA), Event stamp (16:23:18.682 25/10/12), Version (0.4.11), Encoding (BIC/EVENT_SEQ), Qualifier, and Analysis flags (NORMAL).
- SUMMARY:** Provides a high-level overview, including 'pmAnalysisModuleVersion' (0.4.11), 'Analysis result description' (First USR_PERMIT change: Ch 11-BLM_MSK: A T -> F on CIB.SR7.S7.B2), 'Triggered BIC inputs' (Ch 11-BLM_MSK(S7.B2), Ch 11-BLM_MSK(S7.B1), Ch 2-LBDS-b2 (TSU)(R6.B2), Ch 2-LBDS-b1 (TSU)...), 'Beam 1 propagation delay to LBDS' (26000 ns), 'Beam 2 propagation delay to LBDS' (27000 ns), and 'OVERALL' (38 BICs triggered valid PM data).
- EVENT OVERVIEW:** A table listing individual events with columns for Index, Loc. Permit A/B, Time, Delta(uSec), Description, and BIC name. The events are sorted by time, starting from 16:23:18+682038.
- SOURCE OVERVIEW:** A table listing sources with columns for Index, Source Name, and Data Valid. Sources include CIB.UJ56.R5.B1, CIB.UA83.L8.B2, CIB.UJ56.R5.B2, CIB.SR7.S7.B1, CIB.UA83.L8.B1, CIB.US15.L1.B1, CIB.US15.L1.B2, CIB.SR7.S7.B1, CIB.SR7.S7.B2, CIB.UA63.L6.B1, CIB.USC55.L5..., CIB.UA87.R8..., CIB.UA87.R8..., CIB.UA63.L6.B2, CIB.USC55.L5..., CIB.US15.R1.B1, CIB.US15.R1.B2, CIB.UJ33.U3.B2, CIB.UJ33.U3.B1, CIB.UA63.L6.B2, CIB.UA67.R6.B1, CIB.UA67.R6.B1, CIB.UA63.L6.B1, CIB.SR8.INJ2.1, CIB.SR3.S3.B1, CIB.SR2.INJ1.1, CIB.SR2.INJ1.1, CIB.UA67.R6..., CIB.SR2.INJ1.2, CIB.UA67.R6..., CIB.UA23.L2.B2, CIB.CCR.LHC.B1, CIB.UA47.R4..., CIB.UA47.R4..., CIB.UA23.L2.B1, CIB.CCR.LHC.B2, CIB.UA43.L4.B2, CIB.UA43.L4.B1, CIB.T276.U7.B2, CIB.T276.U7.B1, CIB.SR8.INJ2.2, and CIB.UA37.B2.
- FILTER:** A section at the bottom with checkboxes for various event types: Beam_Permit_Loop, Beam_Permit, Local_Permit, User_Permit, User_Permit_Glitch, Software, Mask, Masked_Permit, Disabled_Permit, Channel_Enable, Test, Power, Self_Test, Time, Safe_Beam_Flag, Marker, Injection BICs, Channel A, Channel B, Beam 1, Beam 2, and Generator.

60A interlock implementation

- **No hardware interlocks** for 60A orbit correctors
- Protection **guaranteed by Power Converters**
- Interlocks **to avoid unnecessary quenches** of magnets and current leads and to help operations
- **PC_PERMIT_60A** derived from cryogenic and powering conditions and **sent via GMT** to EPC gateways



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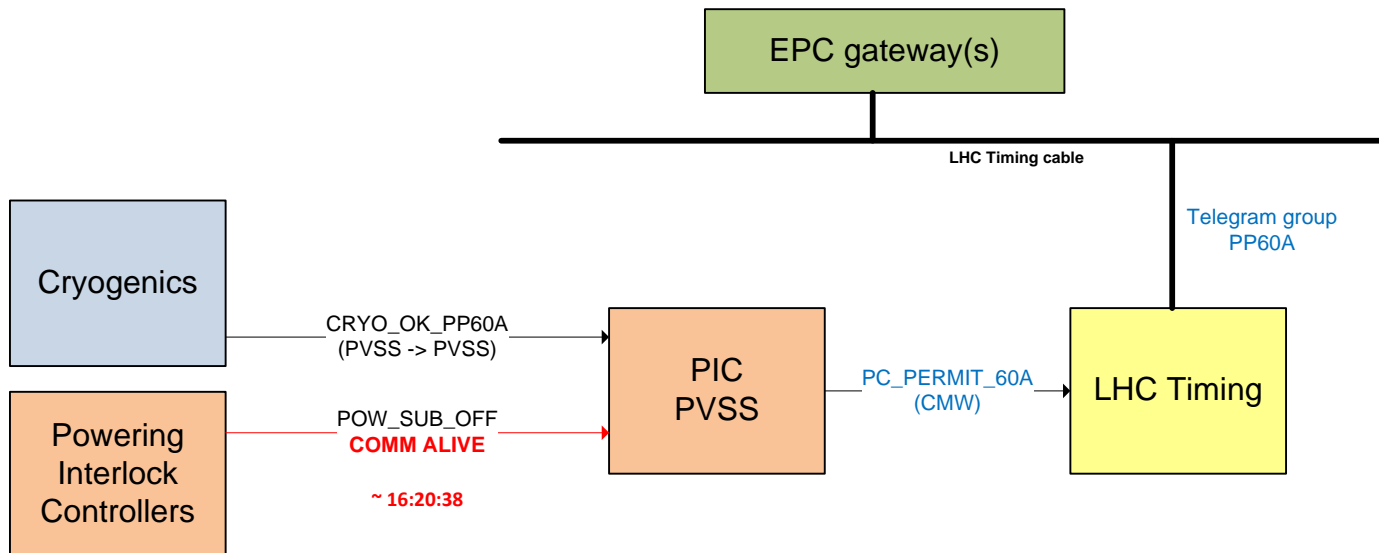
TECHNET of type Universe

Information Interfaces Neighbors Alarms Events

Show

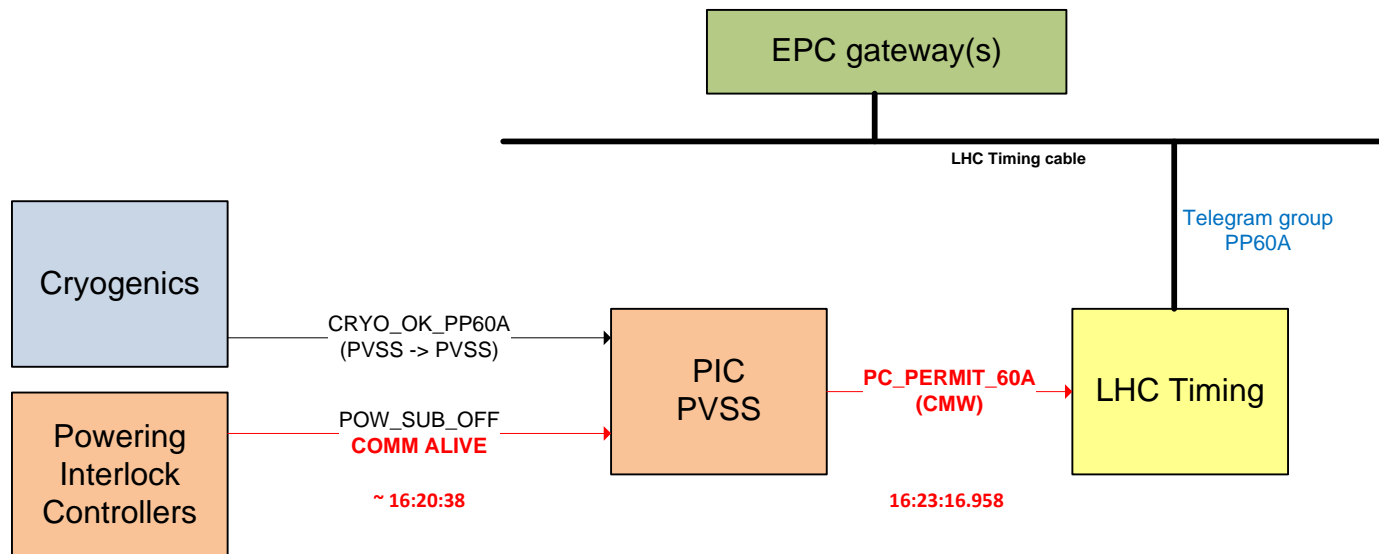
1556 event(s) from 25-Oct-2012 13:00:00 CEST - 25-Oct-2012 19:00:00 CEST

Severity	Created On	Name	Event	Created By	Cleared On	Cleared By
	25-Oct-2012 16:20:38 CEST	p2613-1-ipz-s3c44-1	hpicUsrAuthWMAFailVlan = 1 hpicUsrAuthWMAFailPort = 4 hpicUsrAuthWMAFailMAC = 00:0e:8c:f7:52:86 Alarm number 2433065 with probable cause id 0x10701 generated for device p2613-1-ipz-s3c44-1 of type 3Com44xx. The severity of this alarm is MAJOR.	System		
Major	25-Oct-2012 16:20:38 CEST	p2613-1-ipz-s3c44-1	Device p2613-1-ipz-s3c44-1 of type 3Com44xx is no longer responding to primary management requests (e.g. SNMP), but appears to be responsive to other communication protocol (e.g. ICMP). This condition has persisted for an extended amount of time. An alarm will be generated. An "hpicPortSecAuthFailure" event has occurred, from HPProCurve device, named n212-1-n5-shn2-1.	System	25-Oct-2012 16:26:11 CEST	System



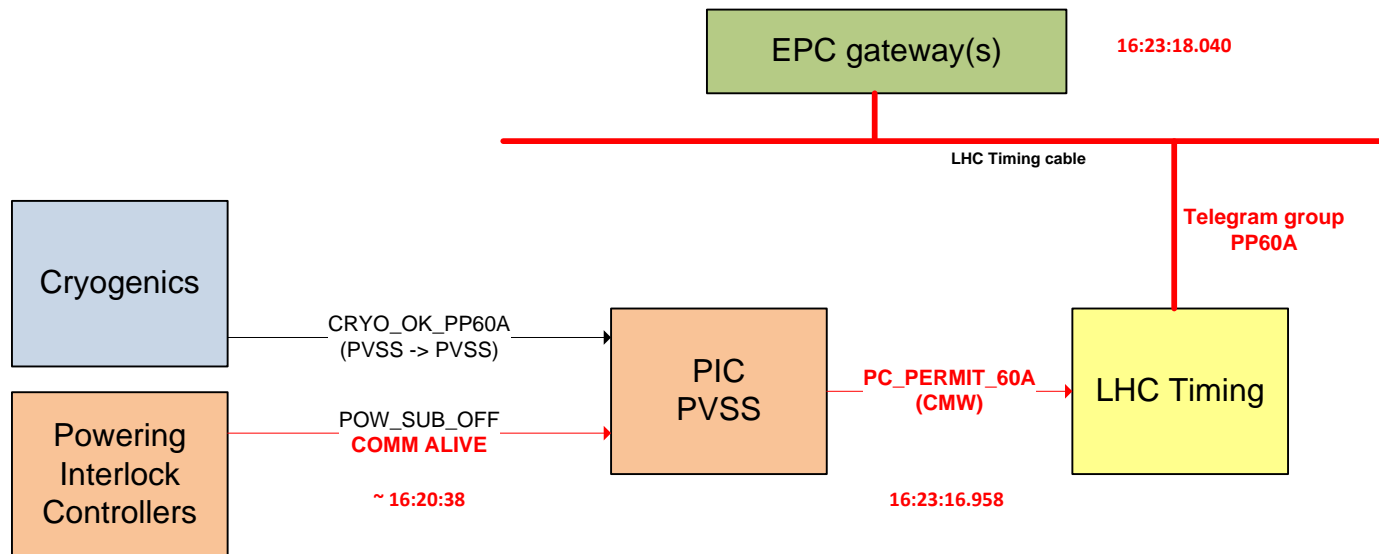
Beam dump after losing PP_60A

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 - 16:23:16.958 => Loss of the PC_PERMIT_60A in sector 56



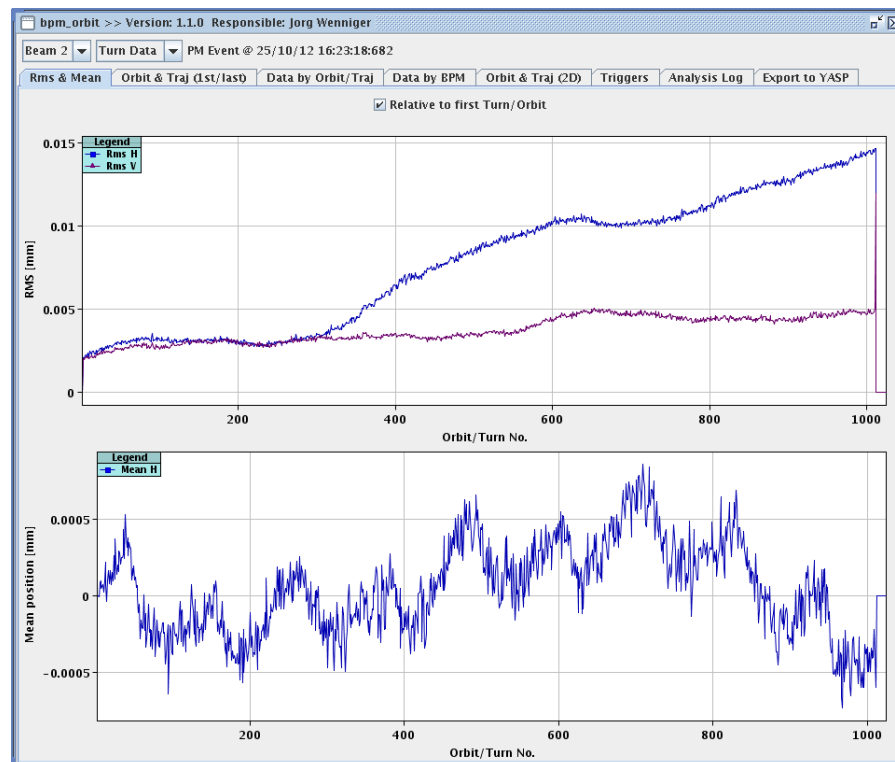
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 - 16:23:18.040 => Slow power abort received by 60A Power Converters

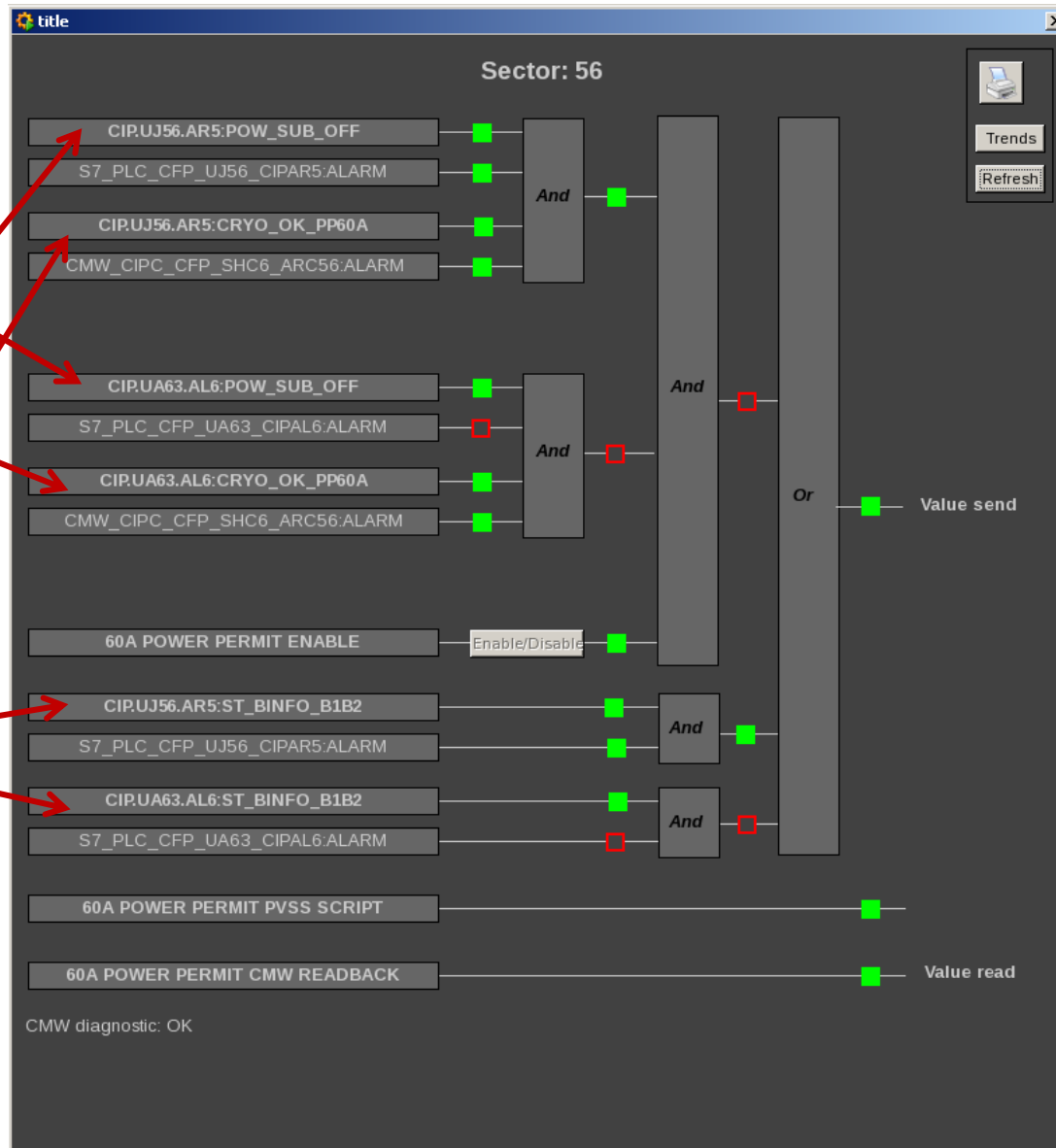


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 - **16:23:18.685 => Beam orbit affected and beams dumped by BLMs in SR7**



What we saw in PVSS...

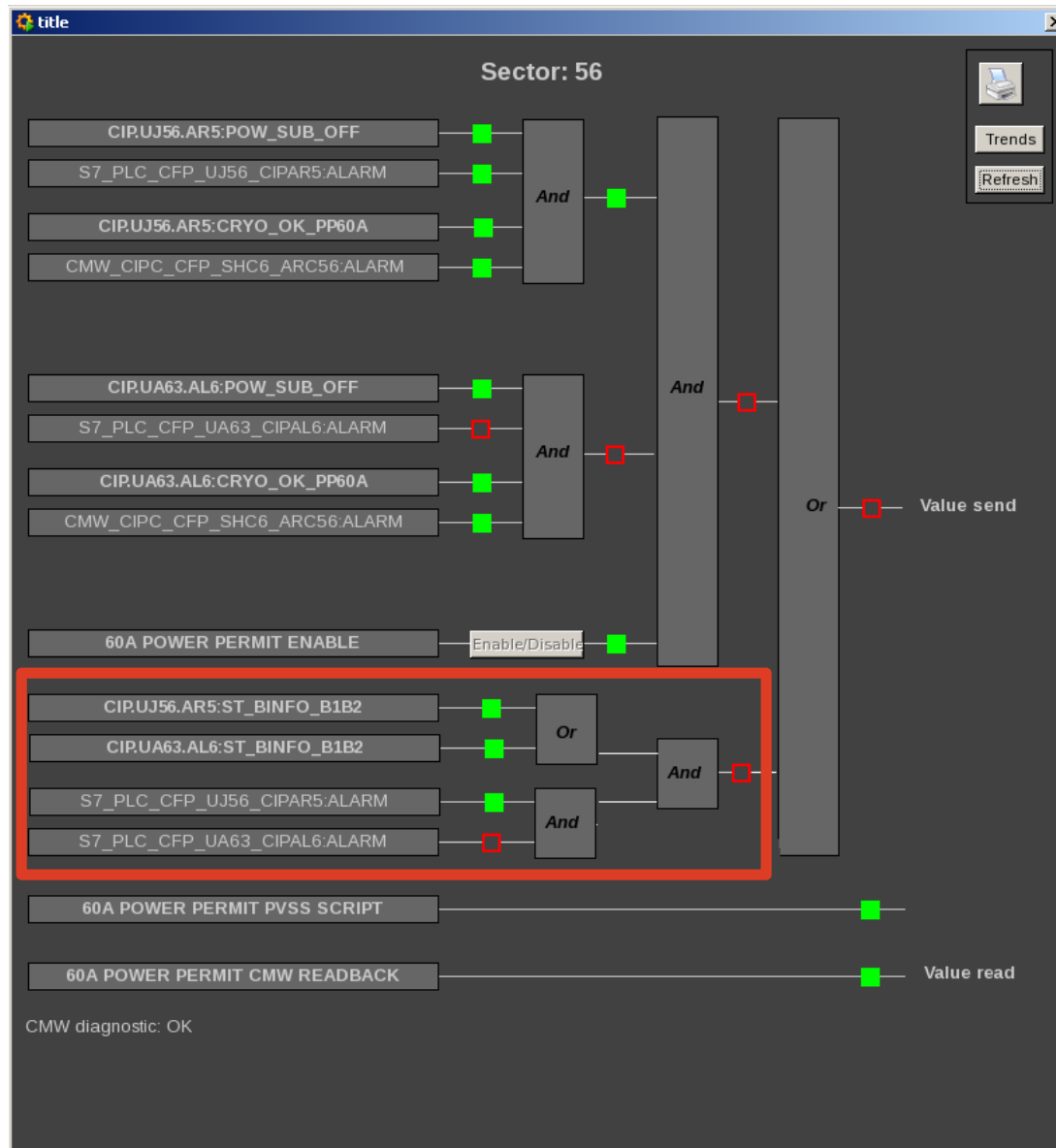


Powering subsector OFF

Cryo conditions 60A

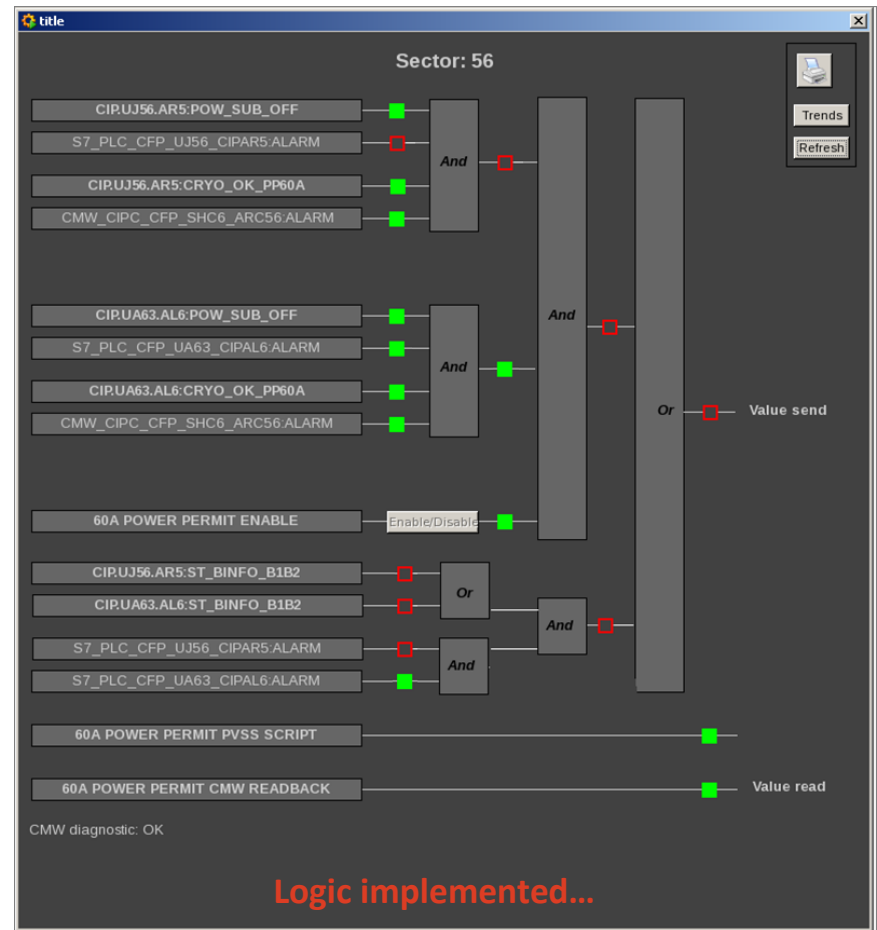
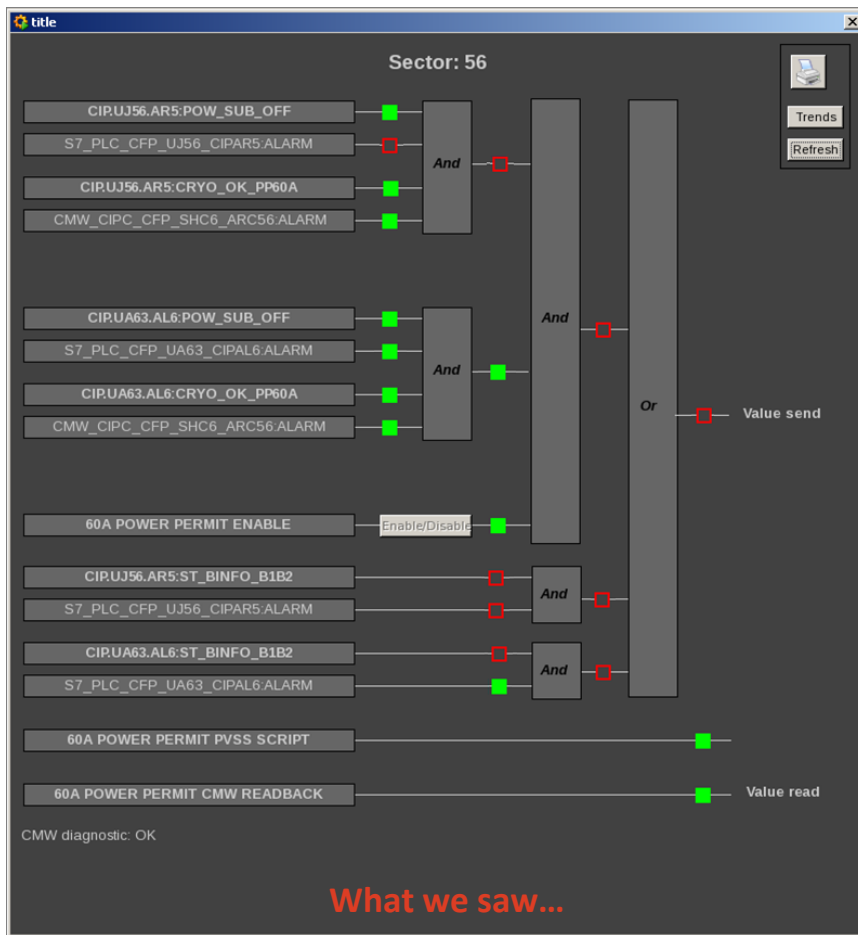
Beam info

But logic implemented...



Similar events without beam...

- 9.04.2010 2h25 / 19.06.2010 11h54 (Sector 56)
 - Network communication problem again in S56
 - This time without beam in the machine...



Conclusions

- Beams would have **never dumped with correct PVSS logic** due to a communication problem affecting a single PIC!!
- PVSS logic will be **corrected during LS1**

- Redundant software interlocks?
 - **1st proposal:**
 - **PC interlocks** not fast enough to detect that situation ($\approx 500\text{ms}$)
 - **PC interlocks** only active (so far) when PC at IDLE, ARMED and RUNNING states

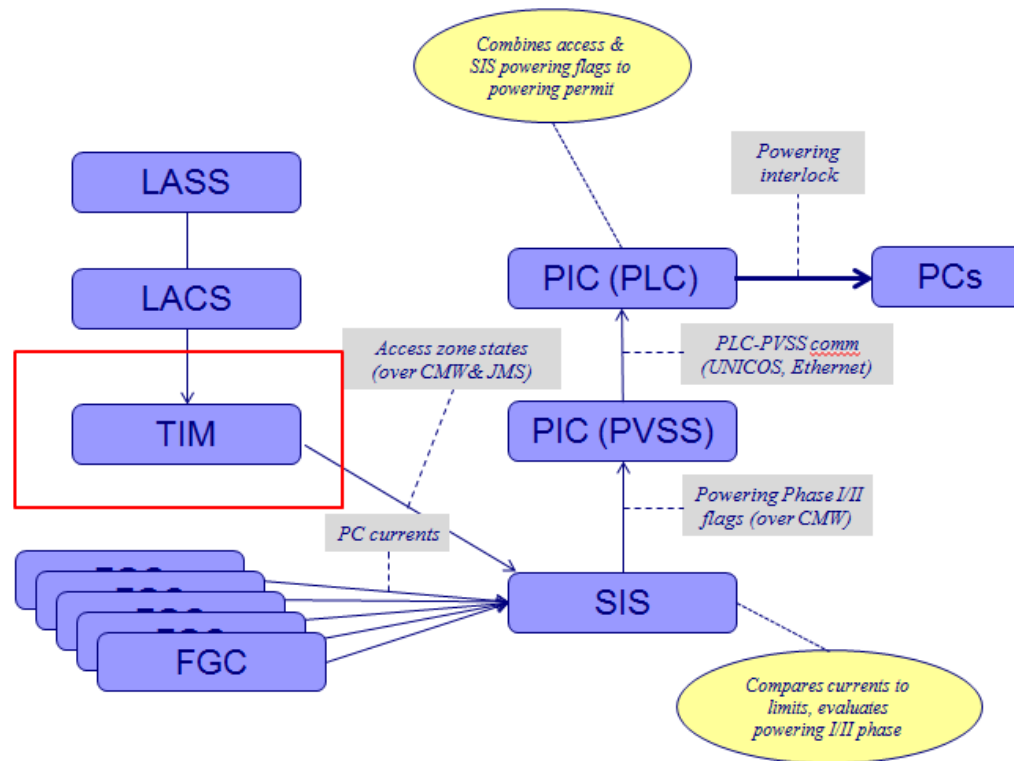
 - **2nd proposal:**
 - **PVSS** could also request a **SLOW POWER ABORT to all PICs** in the sector
 - PIC would also trigger a **beam dump before loss detection**
 - Protection features **cannot depend on PVSS availability**

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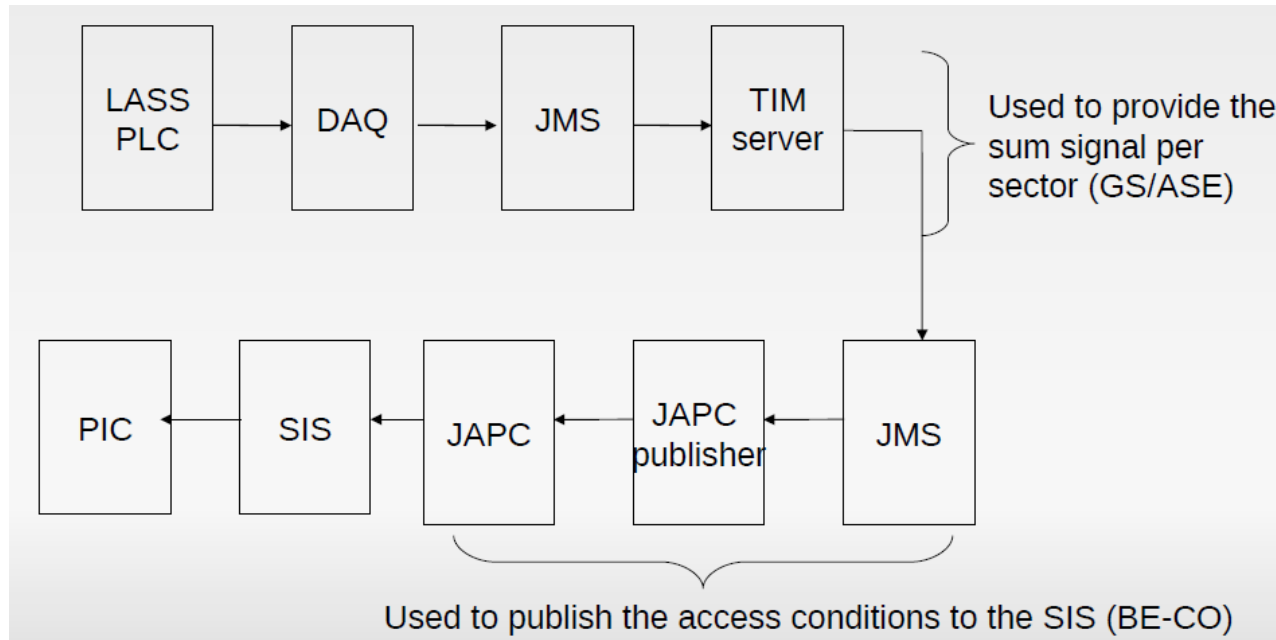
Access Powering Interlocks

- After the incident in September 2008, **new rules for access applied**
- Existing software interlocks **prevent powering above phase I current limit** (1kA all circuits, 100A for RB) and send slow power abort on PIC if needed
- Logic based on a sector-by-sector basis, i.e: 8 independent signals...



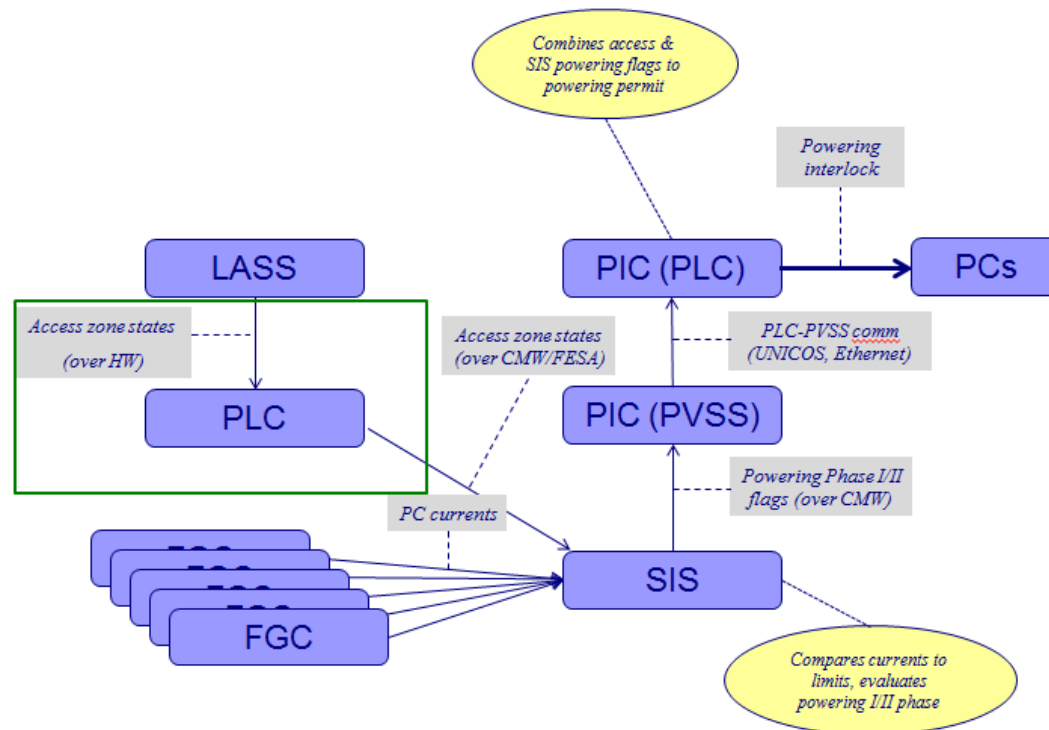
Weakest link...

- Main problem: **Long (unreliable) chain of different SW** components to connect to ACCESS signals
 - Still, **interlock worked always** as expected (fails safe)
 - Improvements done: Masked when BEAM ON
 - Possible further improvements: Shorten SW chain by including JAPC publisher in TIM server



Interlocks renovation

- It requires an **additional PLC** at the PIC side (CCR)
- Communication between **LACS** and **PIC-PLC** via **hardwired signals**
- PIC-PLC will publish access status to **CMW**
- PIC-PVSS will log all access **interlock transitions**
- ECR approved ([EDMS 1246780](#))



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Global protection mechanisms

- Protection mechanisms to **avoid quench propagation** to neighbor magnets
- **Circuit configuration** downloaded to Powering Interlock Controllers
- During **HWC** campaigns such global protection is a **bottleneck for testing!**
- Proposal is to make the Global Protection Mechanism **configurable via PVSS**
- Masking clearly **visible from PIC SCADA system**

PIC SUPERVISION v6.0

LHC Powering Interlocks System

04:26:40 PM 10/09/2012

CIP MASKED INFO

CRYO_START	NOT Masked
CRYO_MAINTAIN	NOT Masked
CRYO_OK_60A	NOT Masked
QPS_OK	NOT Masked
UPS_OK	NOT Masked
AUG_OK	NOT Masked
CRC_OK	NOT Masked

POST MORTEM INFO

TRIGGER	LAST ACQUTC
Multiple triggers	09/10/2012 13:40:40

CIRCUITS INFO

LOCKS	0
SUPER LOCKS	36

SECTOR ACCESS

	S12	S13	S14	S15	S16	S17	S18	S19
PF160A	Permit	Permit	Permit	Permit	Permit	Permit	Permit	Permit
SECTOR ACCESS	Closed	Closed	Closed	Closed	Closed	Closed	Closed	Closed

Param

Pow St

PIC

PIC

PVSS F

Interna

Calcul

Select

Other activities

- **PIC:**

- R2E relocation of 9 PICs to UL14/16 and UL557
- Re-commissioning of UPS hardware links following UPS renovation

- **FMCM:**

- R2E relocation of 1 FMCM from UJ56 to USC55
- Close collaboration with EPC to improve immunity against electrical network perturbations
- Controls renovation in SPS transfer lines

Thanks for your attention

References:

- 60A Powering Permit lost and beams dumped on beam losses
(<http://issues/browse/TE-MPE-COMS-379>)
- Improvement of transmission dependability for the Power Permit of 60A DOC
(<https://edms.cern.ch/document/944765>)
- ECR-Change of the Interlocking of Powering and Access systems
(<https://edms.cern.ch/document/1246780>)

HX:PP60A

