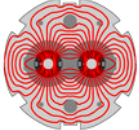




MPP meeting 19/7/2013:

The new BETS on MSI, TDI and
TCDQ

Nicolas Voumard, Jan Uythoven



- Markus reporting on the MPP Workshop in Annecy which took place in March 2013:

Injection / LBDS

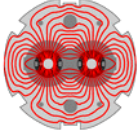
HIGH PRIORITY! Redundant BIS-LBDS retriggering: high reliability required. Reliability run planned for beginning of 2014 (05.2013 -> ongoing in ABT, MPE).

HIGH PRIORITY! TCDIs: virtual beta* and interlocking in SIS via SMP timing. -> Specification (OP, LIBD, Coll).

HIGH PRIORITY! SPS extraction interlocking. ('new' M./Ms. Interlock, OP)

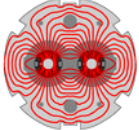
- MSI current, TDI and TCDQ into BETS. Re-do failure analysis. How tight need the tolerances to be? How to mask for setup? (ES in preparation -> LIBD, Coll, MPP)
- TDI gap supervision from SIS to BIS. Redundant gap measurement before LS2 renovation? (EN-STI, MPP)





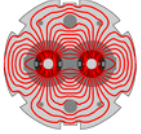
BETS on the Injection Septum MSI

- BETS interlock on absolute MSI current
- Interlock to be connected to maskable LHC Injection BIS input
 - Takes into account the Set-up Beam Flag which moves to unsafe if the NEXT injection from the SPS would make the circulating beam unsafe
 - Same entry to the BIS as the BETS for the TDI presented below
 - The LHC Injection BIS will stop the SPS extraction within a few microseconds
- Proposed tolerances: $7 \mu\text{rad}$ angle = 1σ oscillation = $5e-4$ tolerance on the MSI current ($\sim 0.5\text{A}$)
 - Stability of the MSI current to be checked
- MSI power converter possibly upgraded from mugef to LHC FGC
 - Standard interface for BETS acquisition card
 - Can then ramp down MSI when energy is ramped up



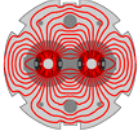
BETS on the Injection Absorber TDI

- BETS interlock on the gap between the jaws.
- Two channels per TDI: one upstream, one downstream
- The threshold function inhibits all injection above and under 450 GeV
- To be connected to maskable input at the LHC Injection BIS, same input as for the MSI BETS interlock will be used
- Proposed tolerance is $\pm 1 \sigma$ on the gap at 450 GeV
 - About +/- 0.6 mm
- Issues
 - No redundant position measurement available
 - Difficult to get present gap measurement with good resolution delivered to the BETS
 - Alessandro's interference project....



BETS on the Dump Absorber TCDQ

- The TCDQ is single sided, interlock on the absolute position
- Two channels per beam: Interlock on upstream and downstream positions
- TCDQ BETS interlock will be connected to an additional maskable channel of the LHC ring BIS
 - Note: the present BETS on the LBDS is connected directly to the TSDS and will remain unchanged



BETS input signals

■ MSI

- 2x 0-10V proportional to MSI current
(main and feedback current measurements)
- 2x DCCT OK signals for status of the power converter

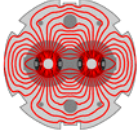
■ TDI – redundant measurement – slides Alessandro

- Manchester encoded frames to be sent directly to BEI
The encoded frame contains Upstream and Downstream jaws spacing. Status of the measurements can be added in the frame.
- Use of NI FlexRIO FPGA customizable boards?



■ TCDQ

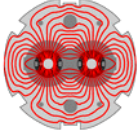
- 2x 0-10V signals from new redundant potentiometers on TCDQ upstream and downstream.
- A 10 V reference for the TCDQ potentiometers is provided by the BETS itself.



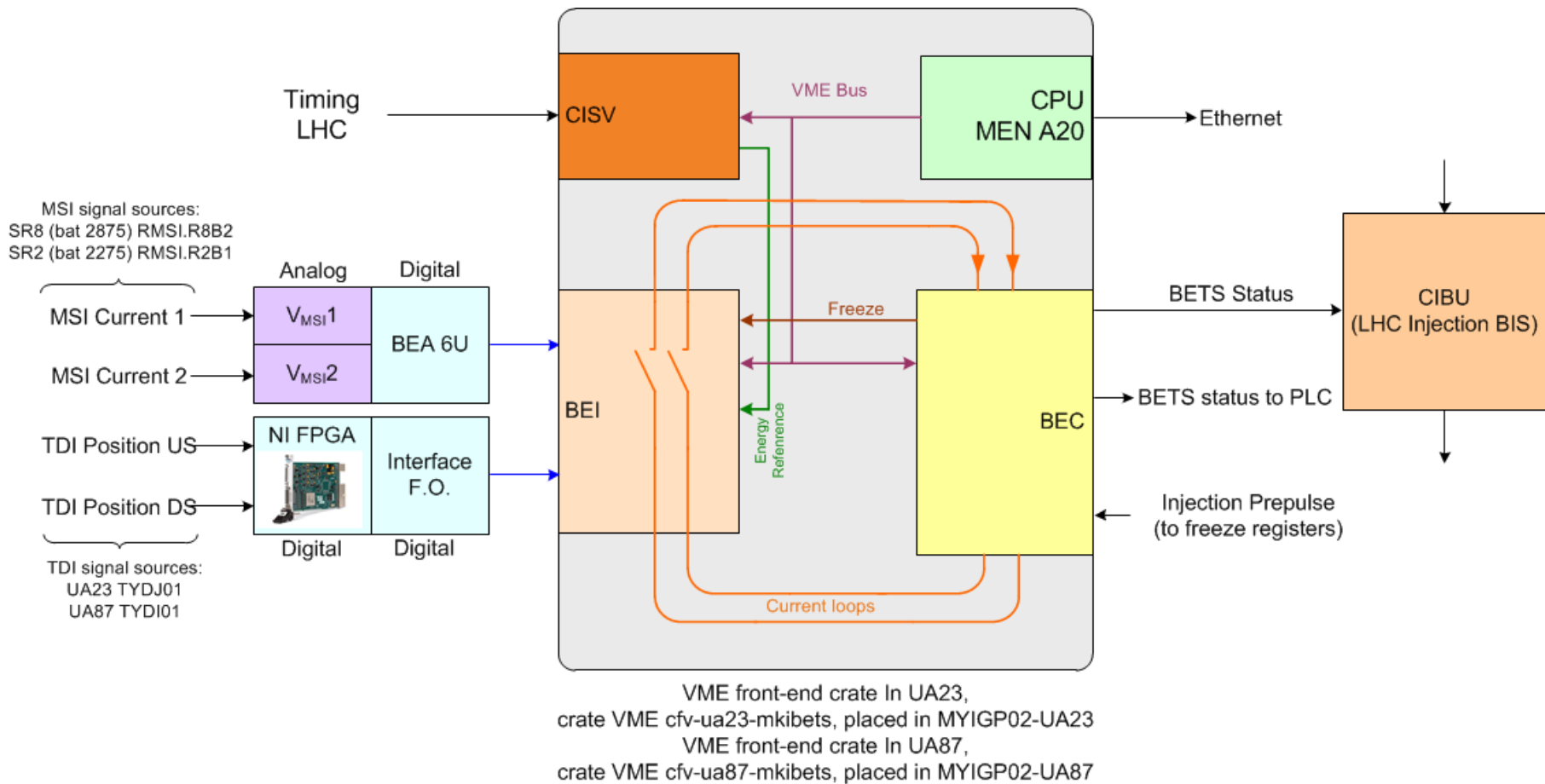
BETS cables and connections

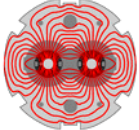
- MSI and TDI
 - MSI and TDI BETS in a single VME crate
 - Additional VME crate to be installed by BE/CO (request done)
 - Connected to LHC injection BIS via standard CIBU (new channels)
 - CIBU crate installation is pending
 - Fiber optics installation request already sent to EN/EL
 - TDI: not a problem as the length is ~20m away from MKI control racks location
 - MSI: possible problem as EPCs are in surface buildings (SR2 & SR8)

- TCDQ
 - BETS installed in a VME crate.
 - Additional VME crate to be installed by BE/CO (request done)
 - Connected to LHC ring BIS via standard CIBU (new channel)
 - Cables to be pulled (can be done by TE/ABT ~30m)
 - Fiber optics installation can be done by TE/ABT (~4m patch)

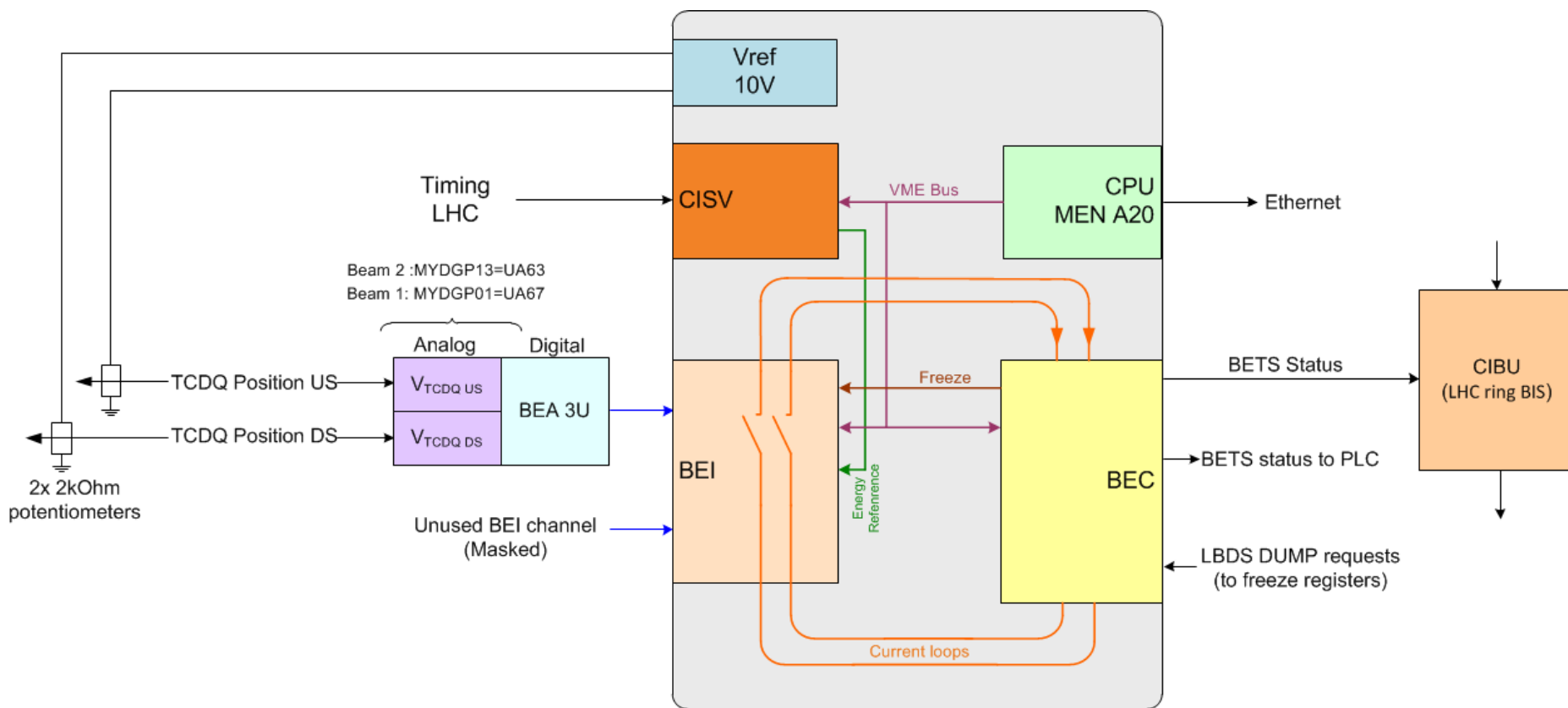


BETS MSI and TDI overview



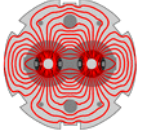


BETS TCDQ overview



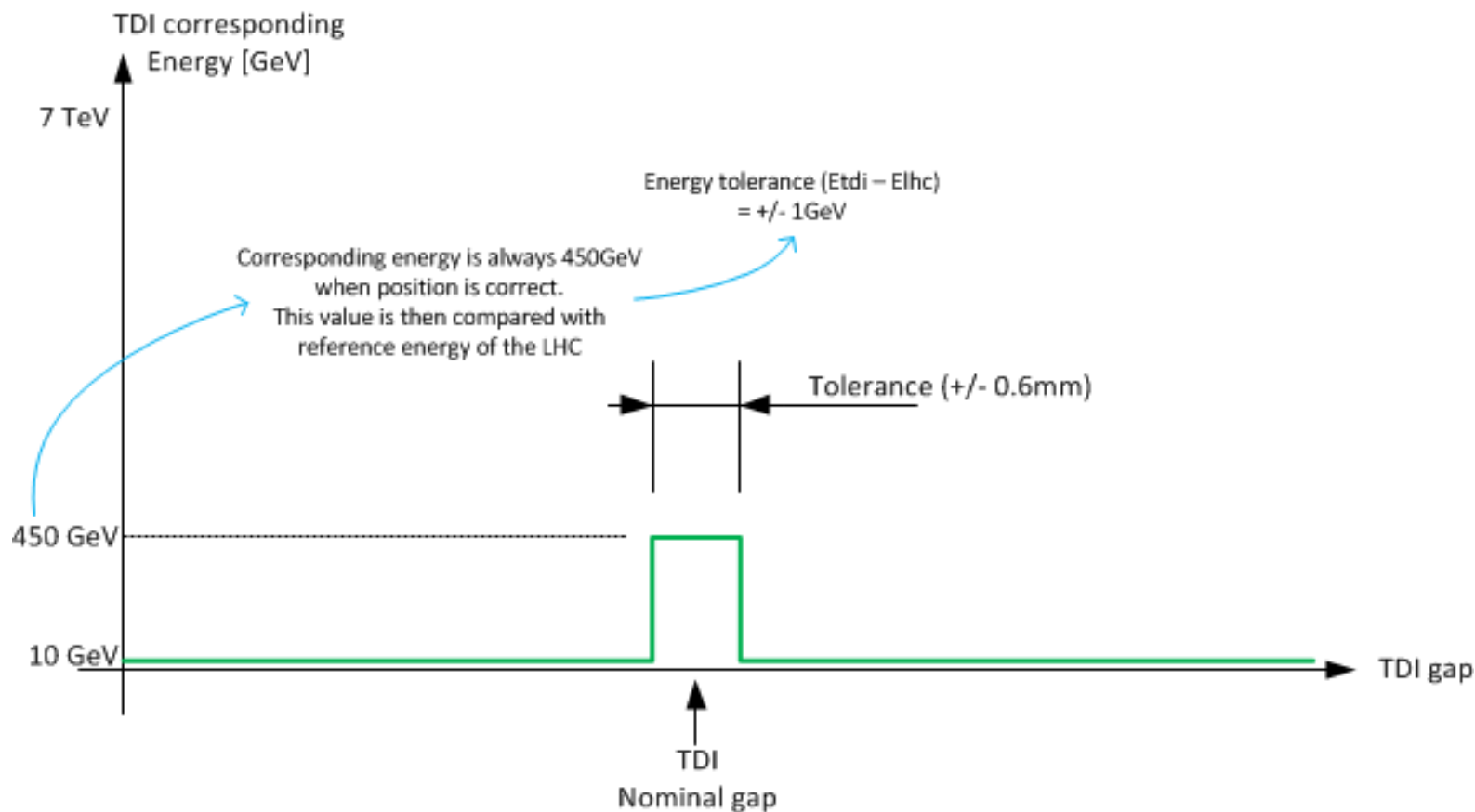
VME front-end crate In UA63,
 crate VME cfv-ua63-tcdqbets, placed in MYDGP08-UA63
 VME front-end crate In UA67,
 crate VME cfv-ua87-tcdqbets, placed in MYDGP06-UA67

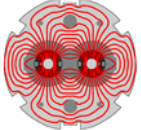




BETS BEI transfer function for TDI

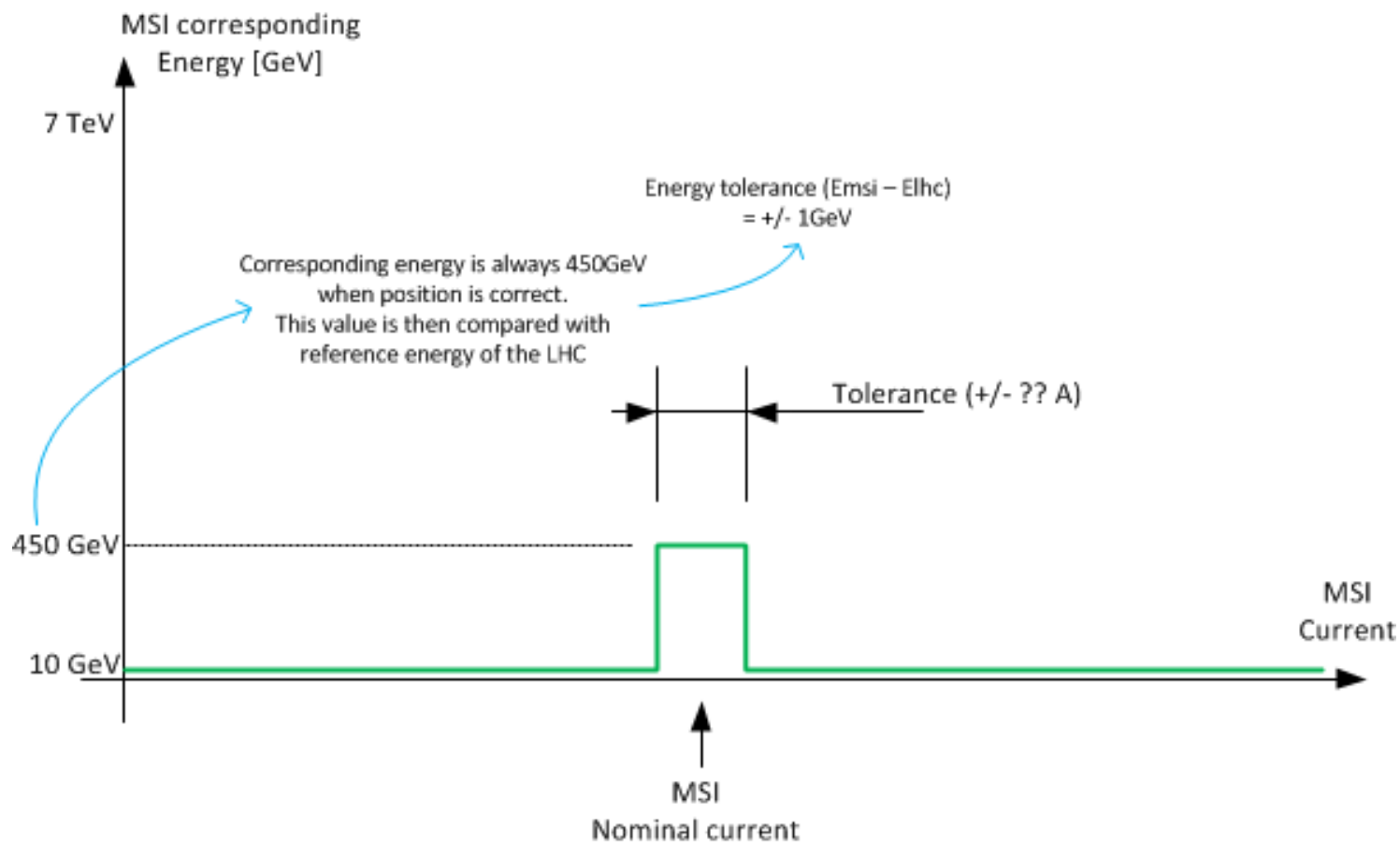
- Change of transfer function to be done locally in the tunnel
- Transfer function to be checked by MCS
- Arming sequence for BETS on TDI not needed (standalone)

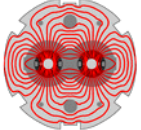




BETS BEI transfer function for MSI

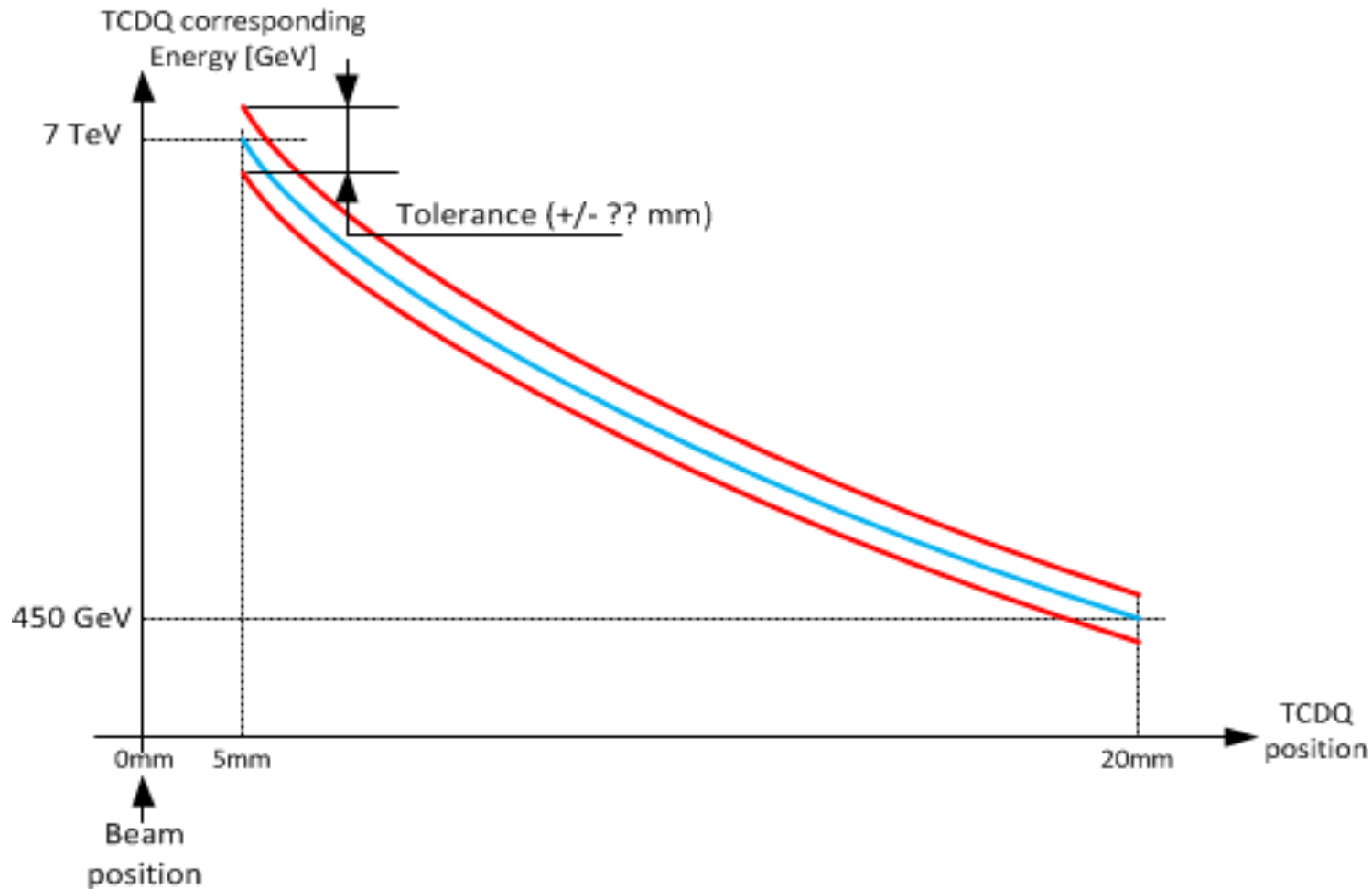
- Change of transfer function to be done locally in the tunnel
- Transfer function to be checked by MCS
- Arming sequence for BETS on MSI not needed (standalone)

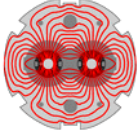




BETS BEI transfer function for TCDQ

- Change of transfer function to be done locally in the tunnel
- Transfer function to be placed in MCS
- BETS on TCDQ needed during the arming sequence of the LBDS





Conclusions

- What is critical ?
 - Fiber optics demands from MSI power converters to BETS not yet confirmed.
 - Status of cabling for additional BIS channels
 - 2 to LHC injection BIS
 - 2 to LHC ring BIS

- What input is missing / decisions outstanding
 - MSI power converter on LHC FGC or not
 - TDI position measurement to be confirmed and financed
 - Functional specification:
 - BETS tolerances and transfer functions
 - Commissioning procedures, etc...