Proposed implementation of redundant BIS-LBDS trigger channel

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Outline

Current configuration

- LHC Beam Permit Loops
- LBDS triggers

New BIS Asynchronous Trigger

Build the link

- Separate the hardware
- The dumping system “Local mode”
- CIBM link to avoid Asynchronous Dumps

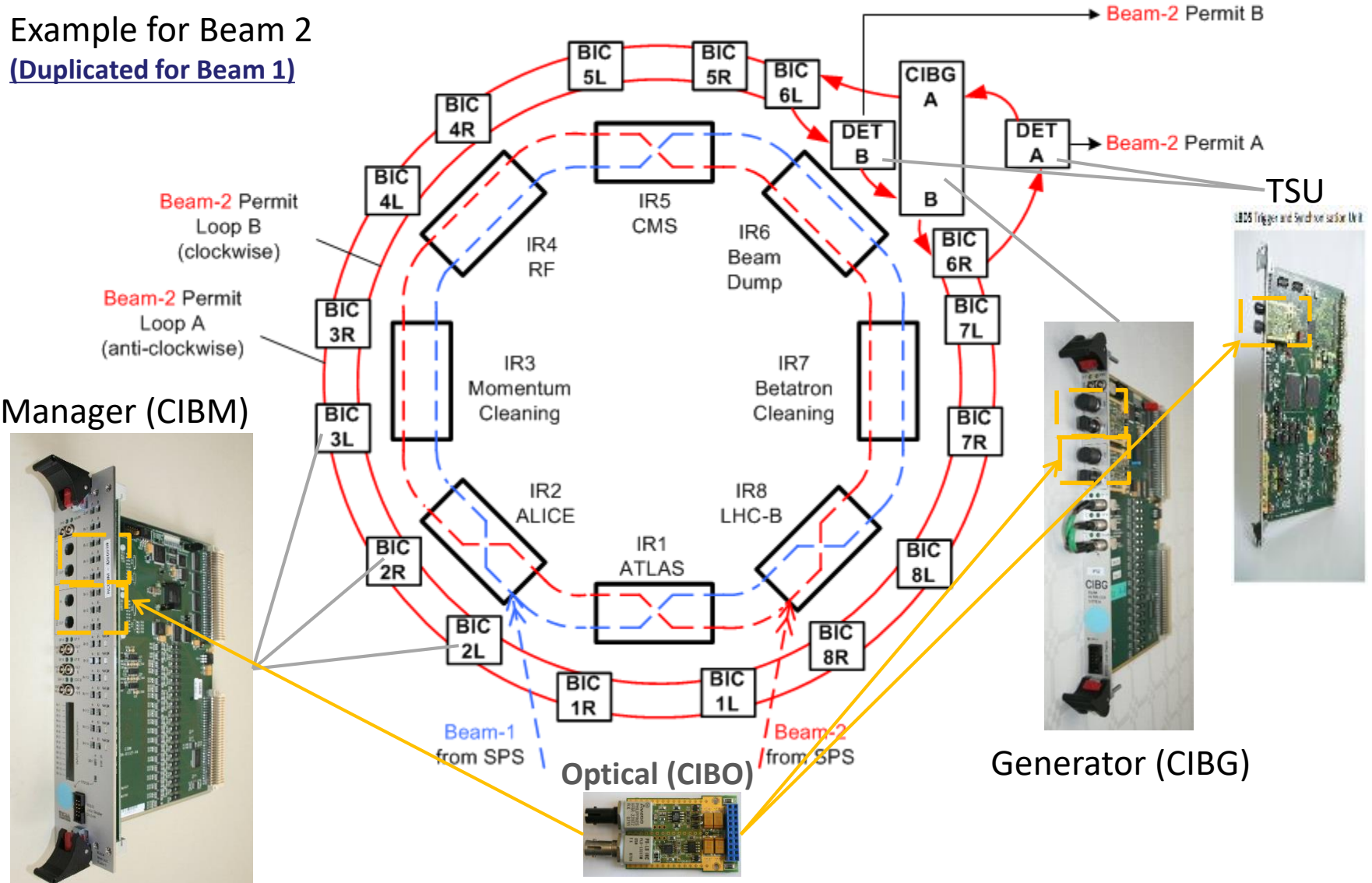
Global layout

Questions

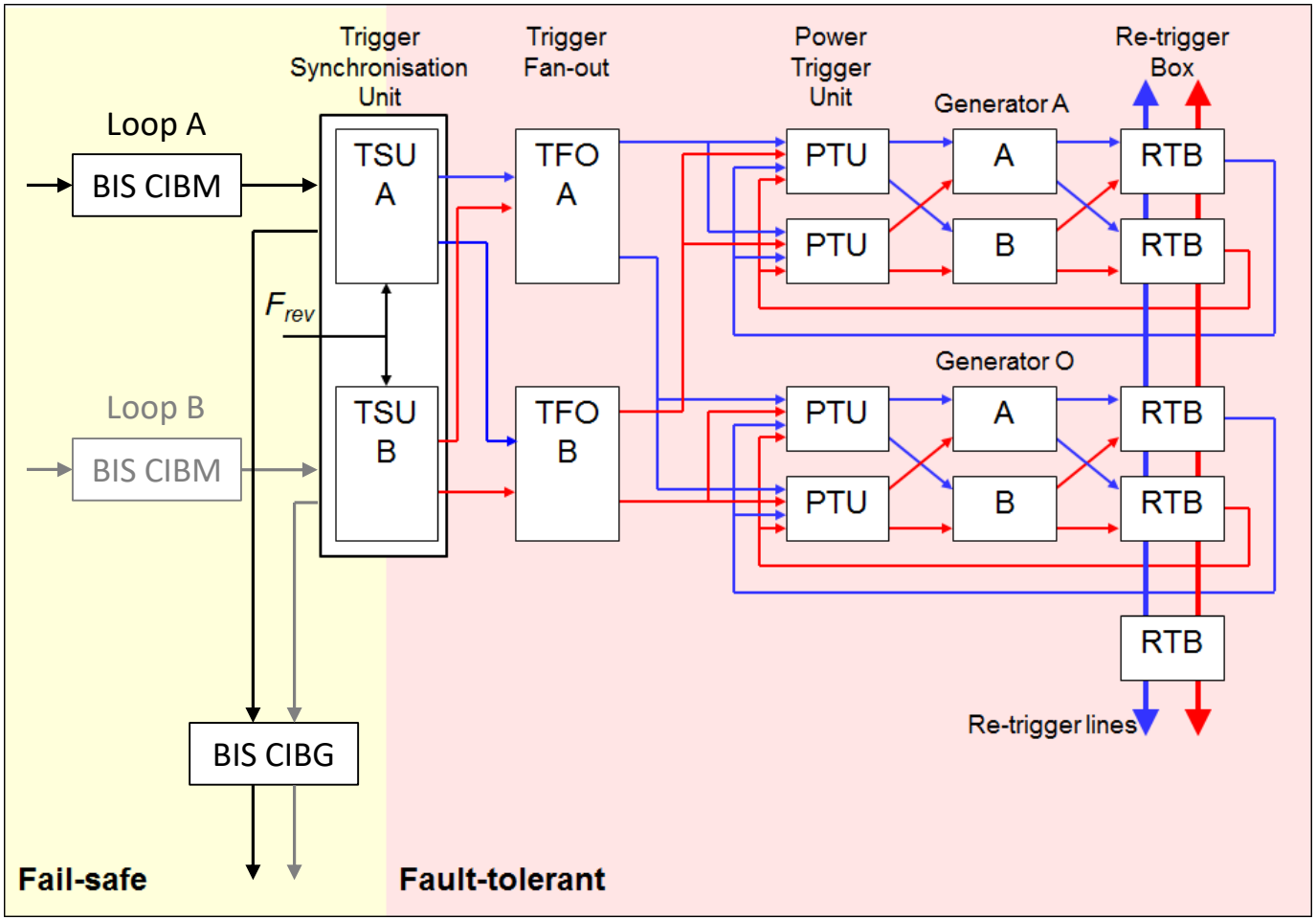
LHC Beam permits loops

Example for Beam 2

(Duplicated for Beam 1)



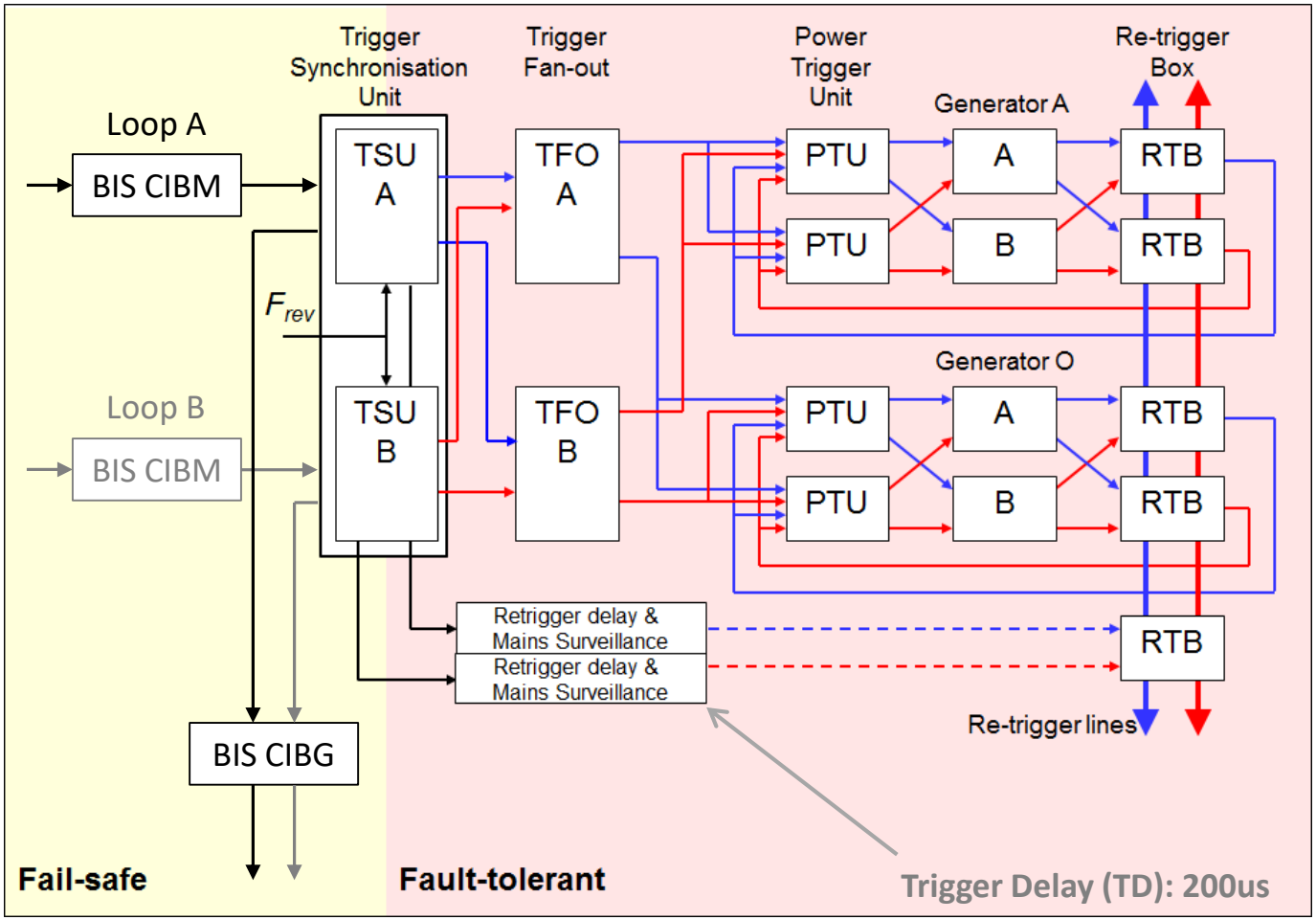
LBDS Synchronous Triggers 1/3



Courtesy E. Carlier

- Fully redundant Synchronous Beam Dump Triggers (SBDT)

LBDS Triggers 2/3



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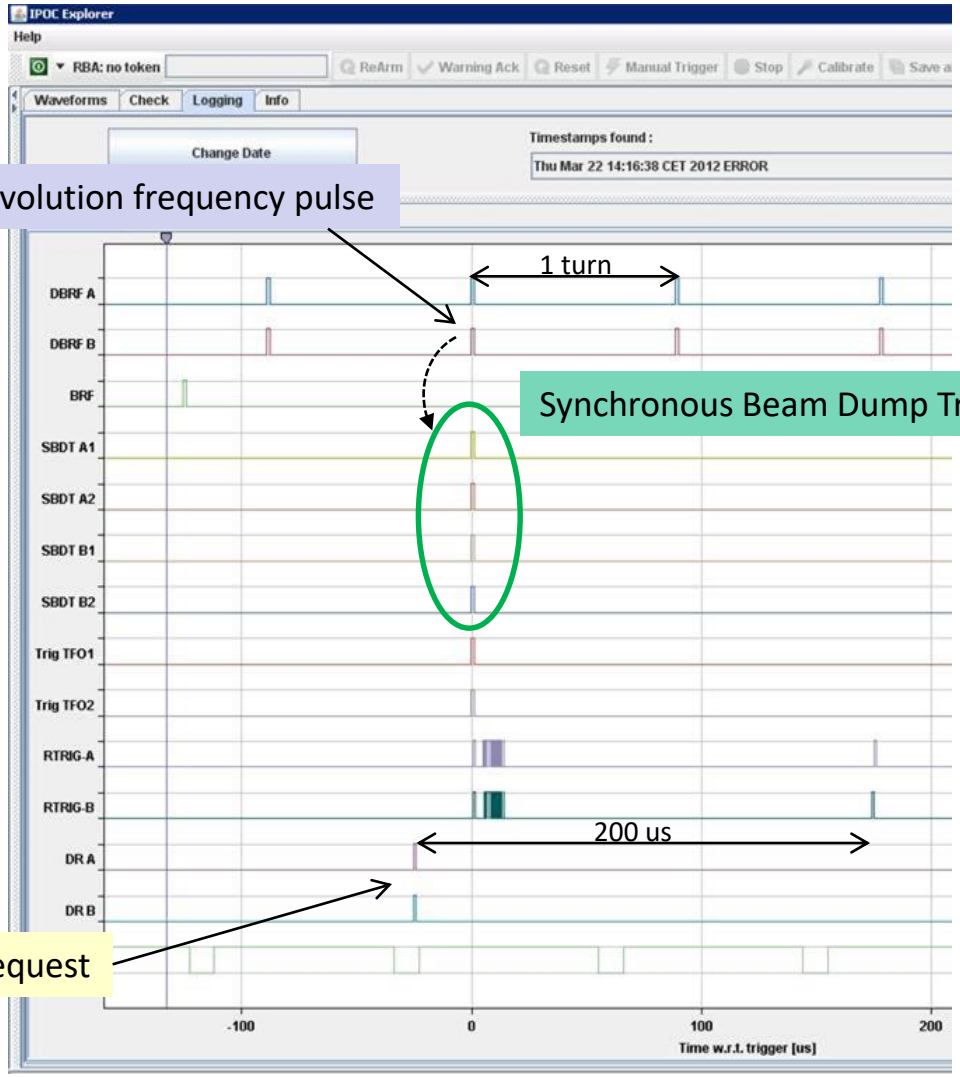
- Fully redundant Synchronous Beam Dump Triggers (SBDT)
- Asynchronous Beam Dump Triggers (ABDT)

LBDS Triggers 3/3



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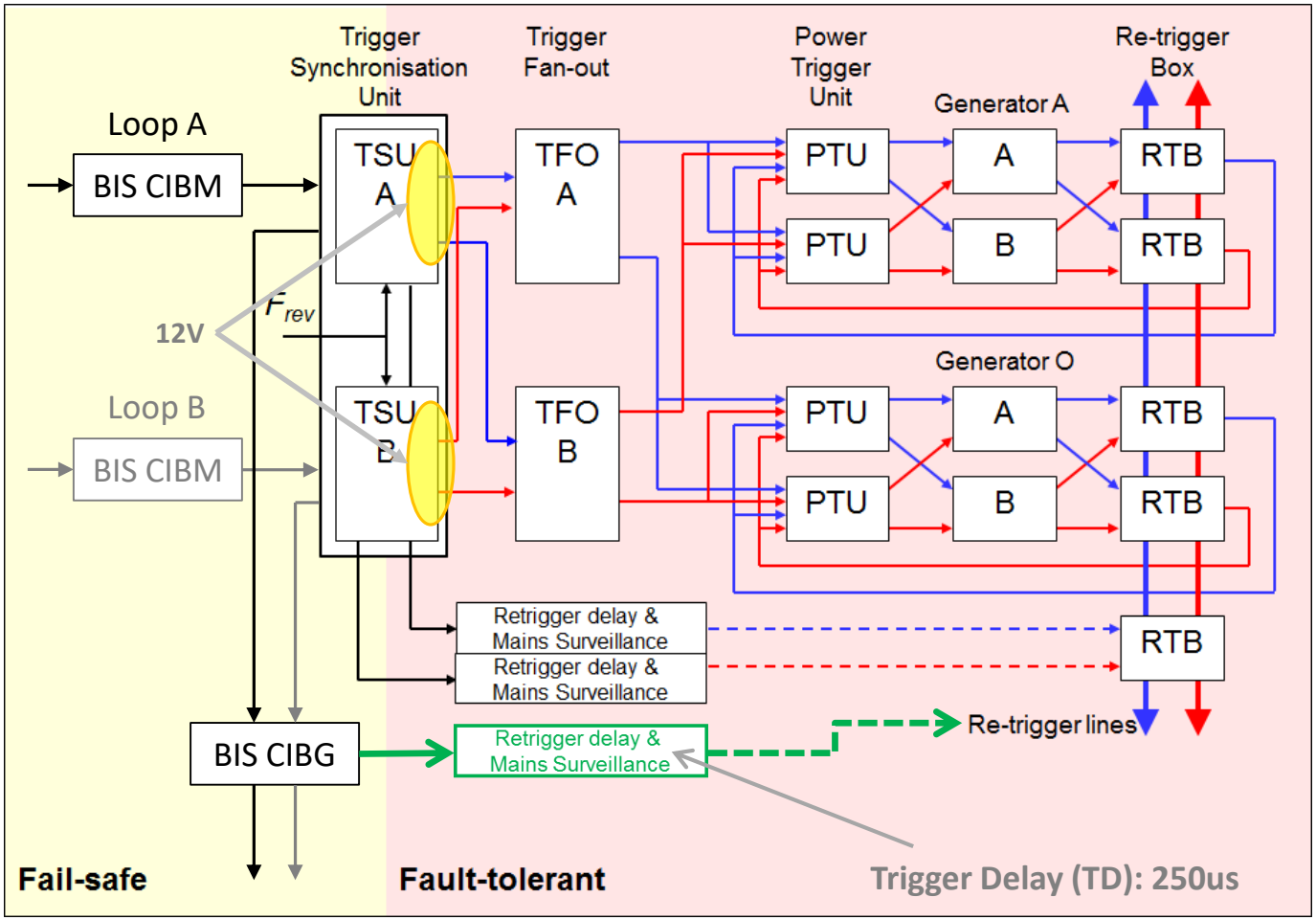
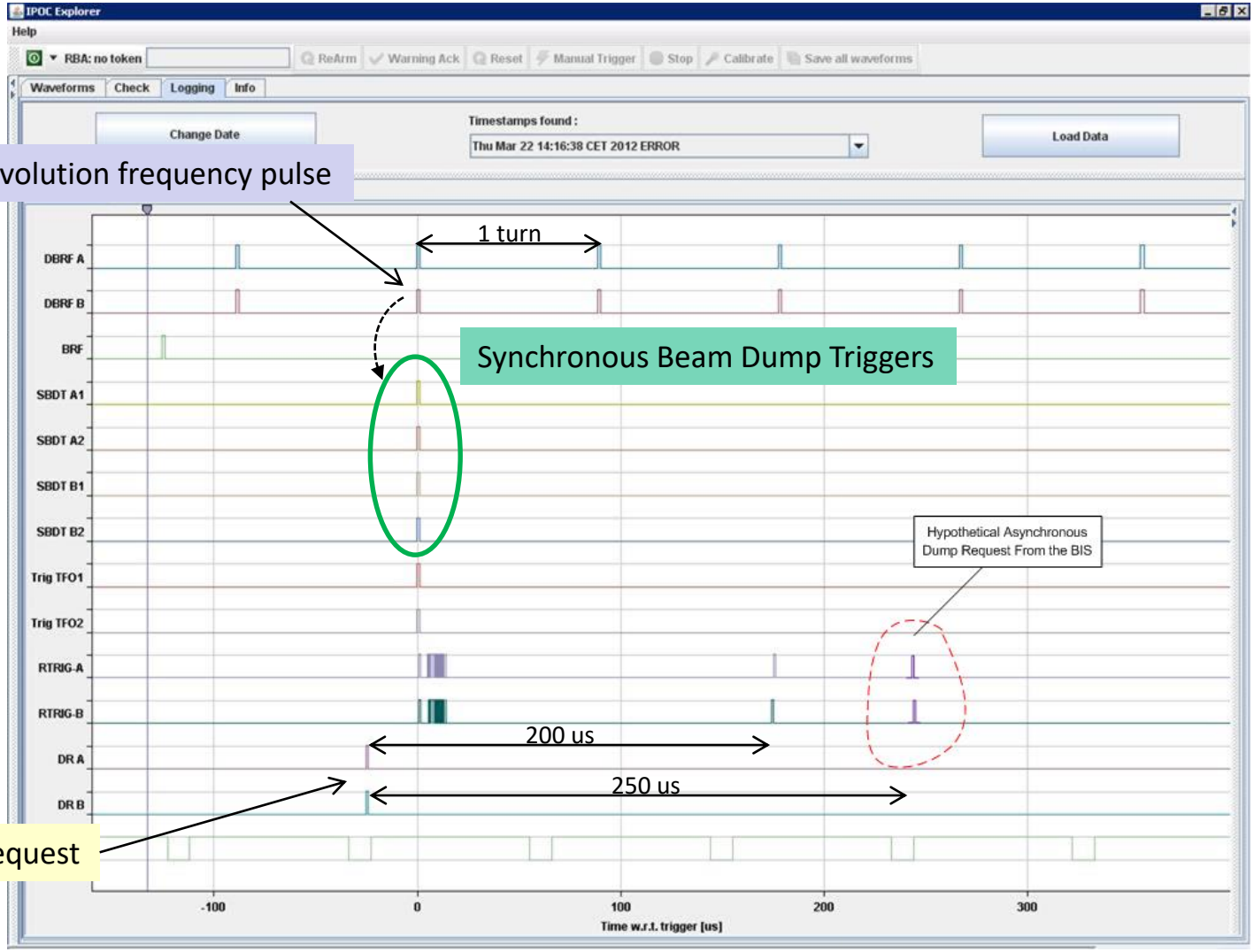
New BIS asynchronous trigger 1/2



- Found a common 12V line on VME bus of the TSU crate (will be solved during LS1)
- Add a link directly from the BIS to the retrigger lines

New BIS asynchronous trigger 2/2



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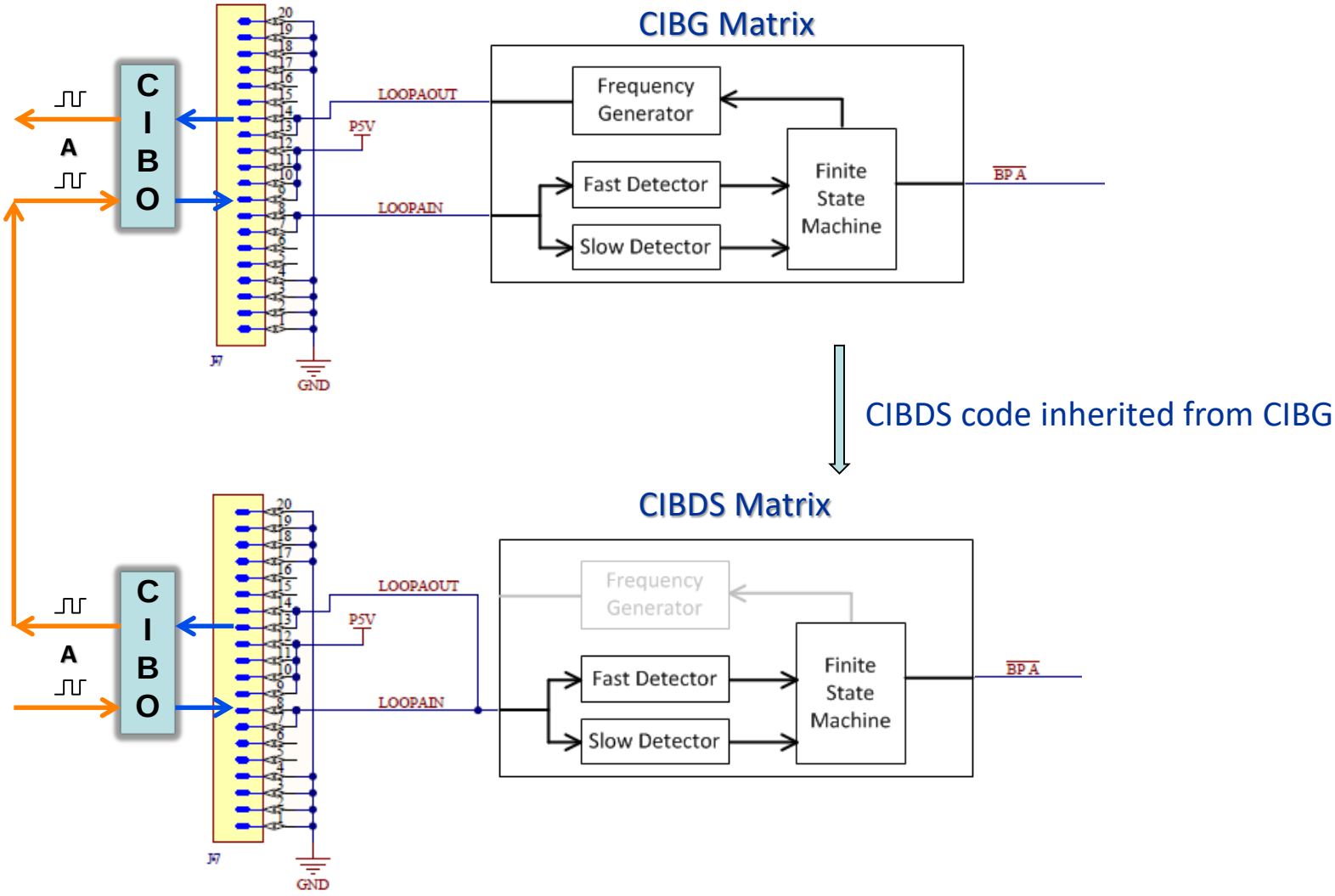
Separate the hardware 1/4

Make a new board means

- Separate the functionalities (CIBG independent)
  - CIBG generates
  - CIBDS* triggers dumps
- No failure induced to the CIBG by changing it
- Duplicate the Matrix code on the CIBDS*

*CIB Dumping System

Separate the hardware 2/4



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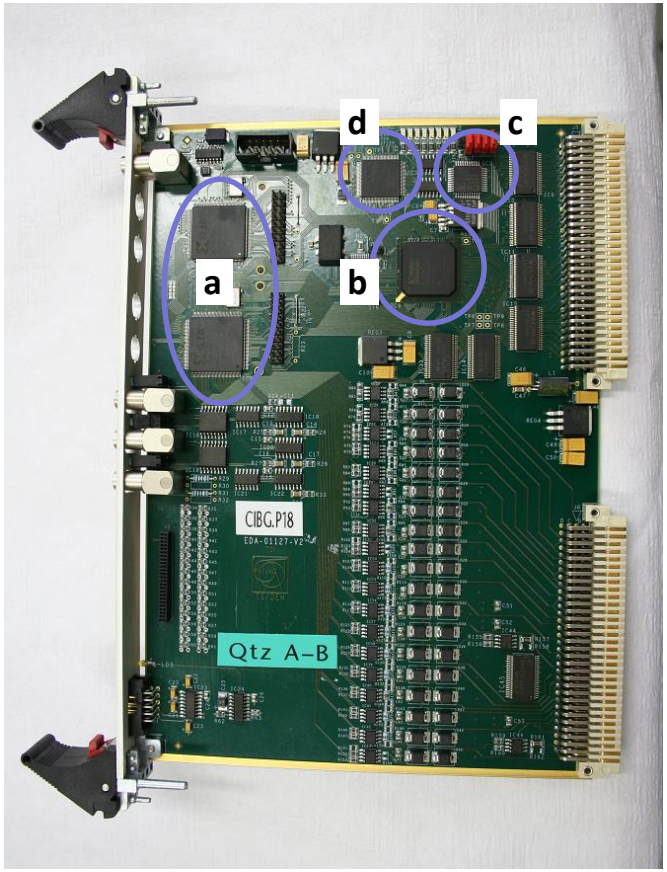
Moreover

- New CIBG does not solve obsolescence problem

*CIB Dumping System

Separate the hardware 3/4

Digital components obsolescence



#	Description	Component	Up to	Price (/100)
a	Critical matrices	CPLD XC95288XL	~2017	25$
b	Monitoring	FPGA Spartan 3	~2018	50$
c	Flash PROM	PROM XC18V04	~2017	25$
d	Remote update	CPLD XC2C128	~2022	25$

⇒ Use of the same hardware and layout

Separate the hardware 1/4

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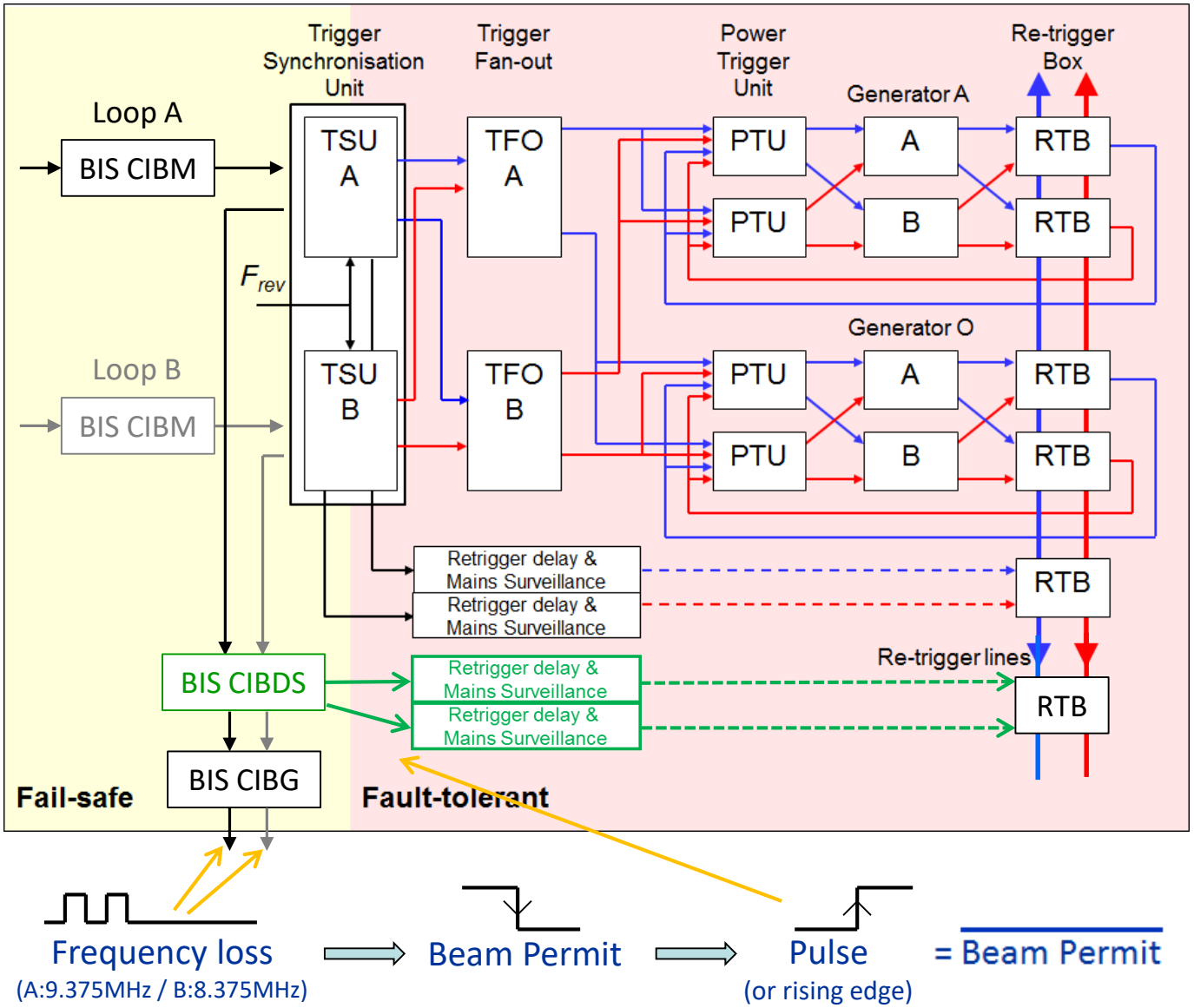
On the other hand

- Special care as we open the BIS optical loops
- A bit more work: new VME connection, FESA, Java, ...
- Take care of obsolescence (Prepare spares to reach LS2)

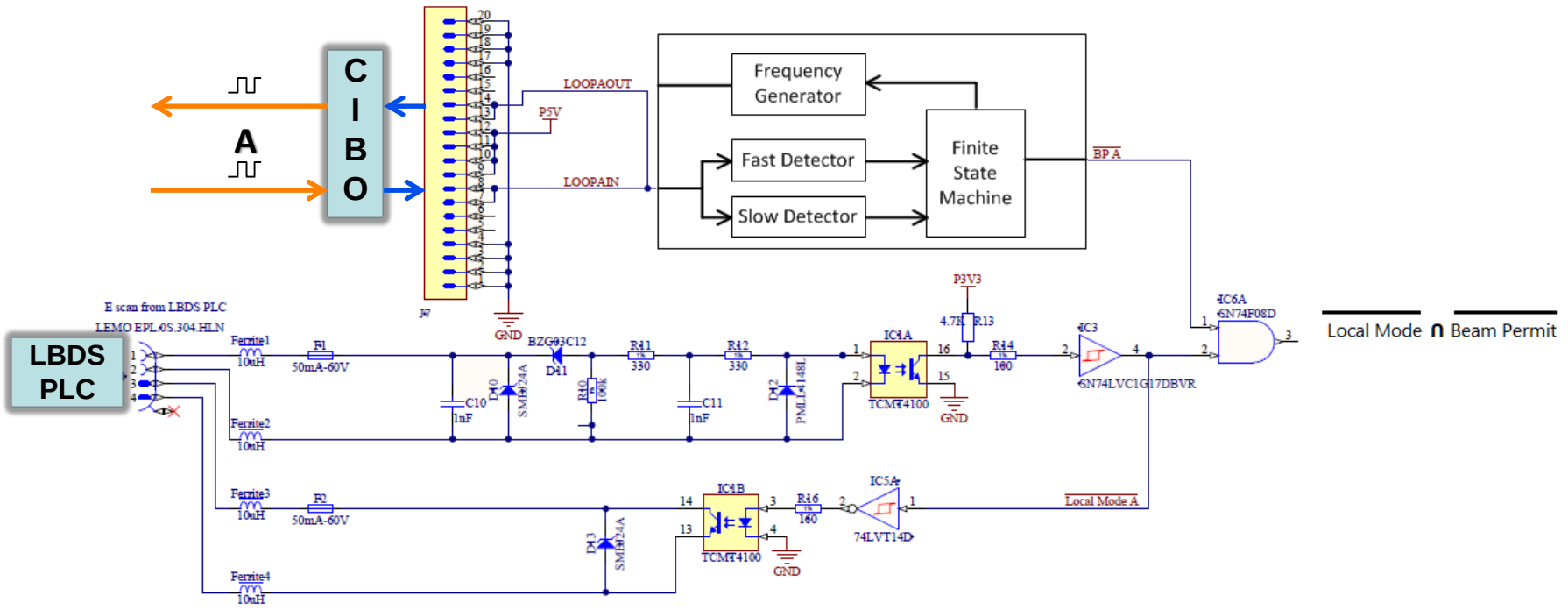
*CIB Dumping System

Separate the hardware 4/4



The dumping system "Local mode" 1/2

- No pulse while LBDS in local mode (not compatible with BIS testing)
- Input from LBDS PLC to inhibit the pulse
- Can be critical
  - ⇒ Read back loop to check the inhibit signal and dump (synchronously) if inconsistency
- Fail safe (no inhibit) in case of cable unplugged



The dumping system "Local mode" 2/2

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Pulse generated if rising edge on the AND gate output

⇔ $\overline{\text{Local Mode}} \cap \text{BP}$ to $\overline{\text{Local Mode} \cap \overline{\text{BP}}}$ => Lose of BP, Normal Dump

⇔ $\text{Local Mode} \cap \overline{\text{BP}}$ to $\overline{\text{Local Mode} \cap \overline{\text{BP}}}$ => Pulse at the end of a Local mode

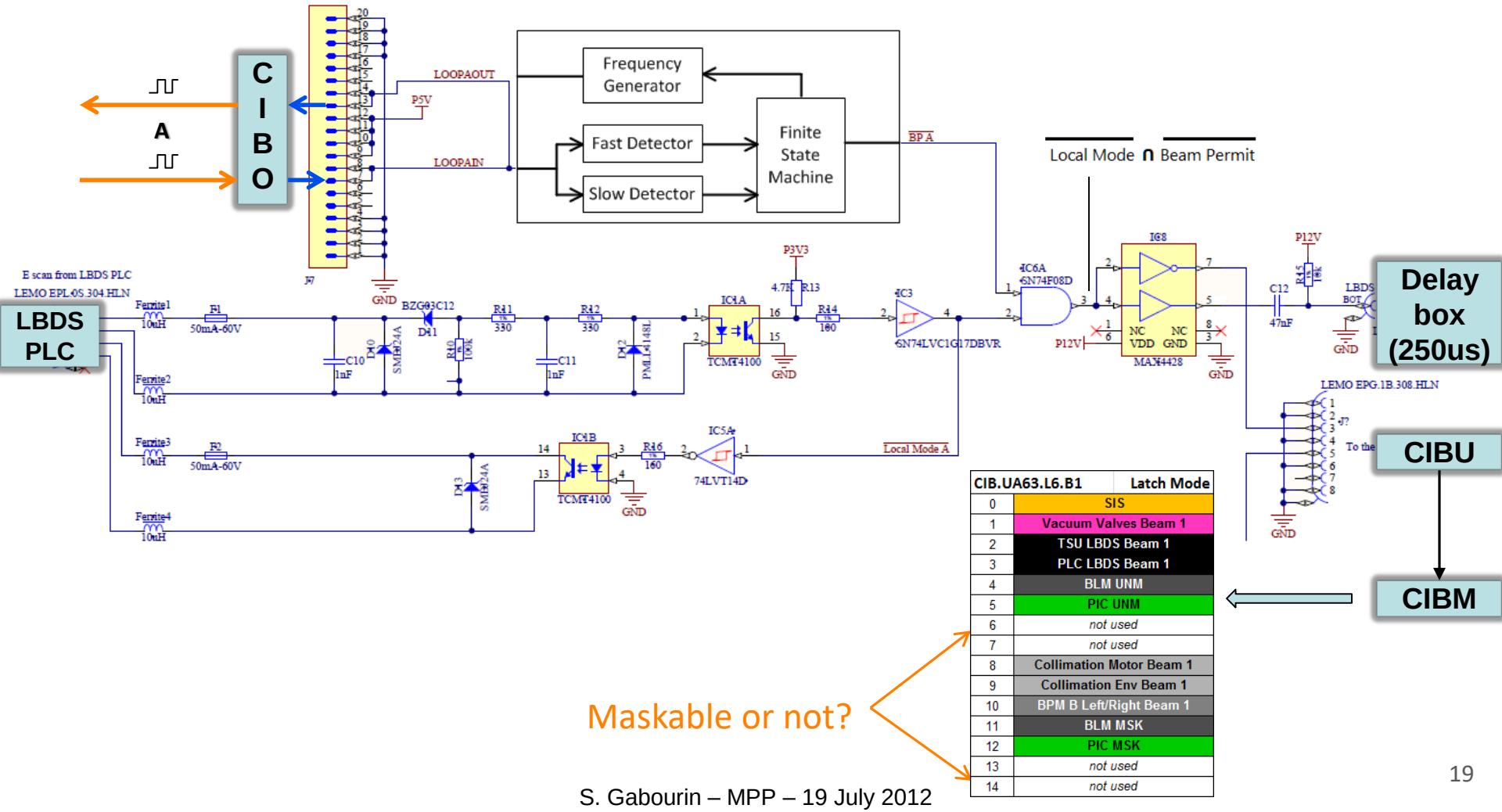
⇓

Can be used as test for the LBDS!

CIBM link to avoid Asynchronous Dumps 1/2

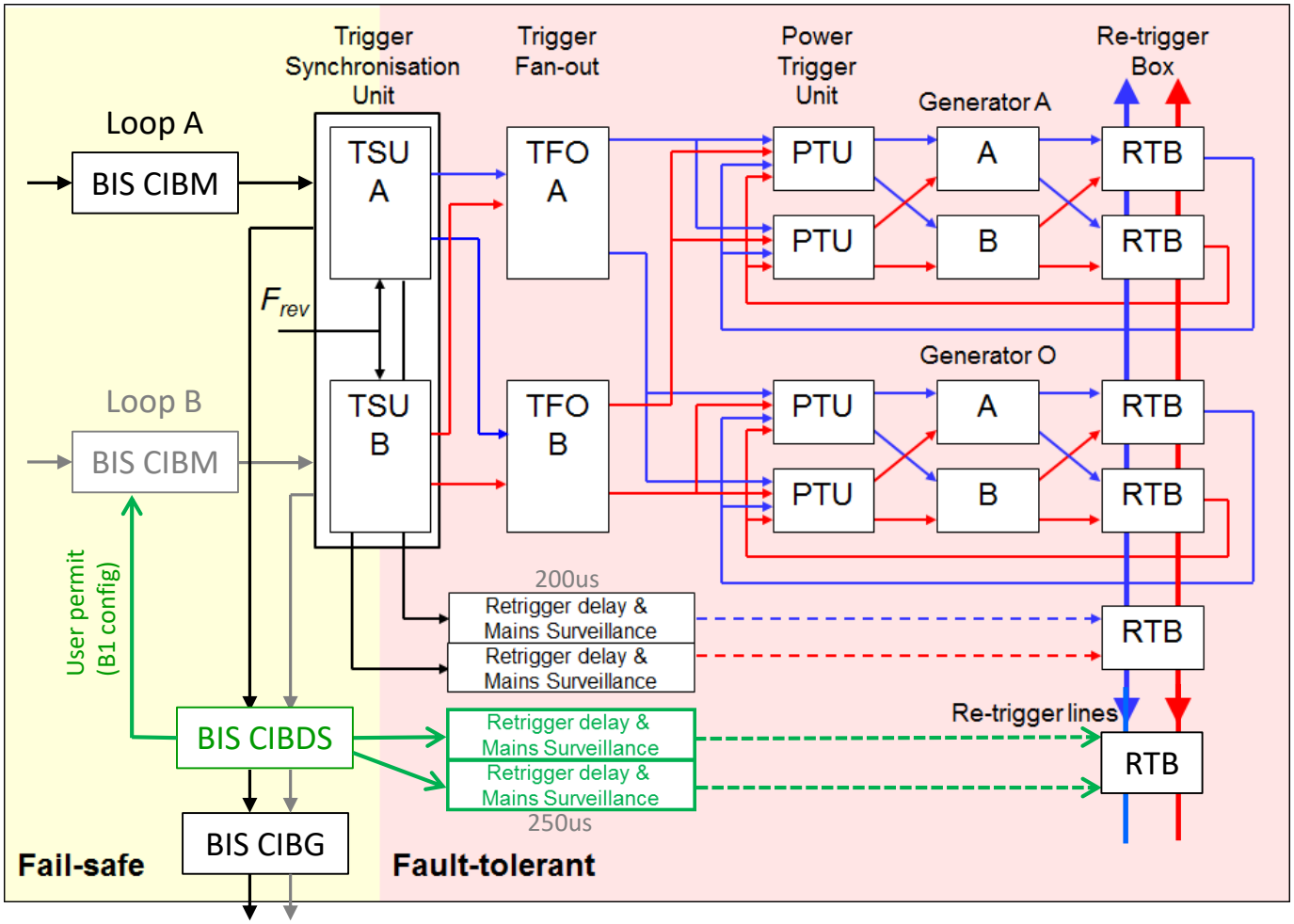
Back loop as User Input of a CIBM

=> Any spurious trigger will initiate Synchronous Dump before the 250us delay



CIB.UA63.L6.B1	Latch Mode
0	SIS
1	Vacuum Valves Beam 1
2	TSU LBDS Beam 1
3	PLC LBDS Beam 1
4	BLM UNM
5	PIC UNM
6	not used
7	not used
8	Collimation Motor Beam 1
9	Collimation Env Beam 1
10	BPM B Left/Right Beam 1
11	BLM MSK
12	PIC MSK
13	not used
14	not used

CIBM link to avoid Asynchronous Dumps 2/2



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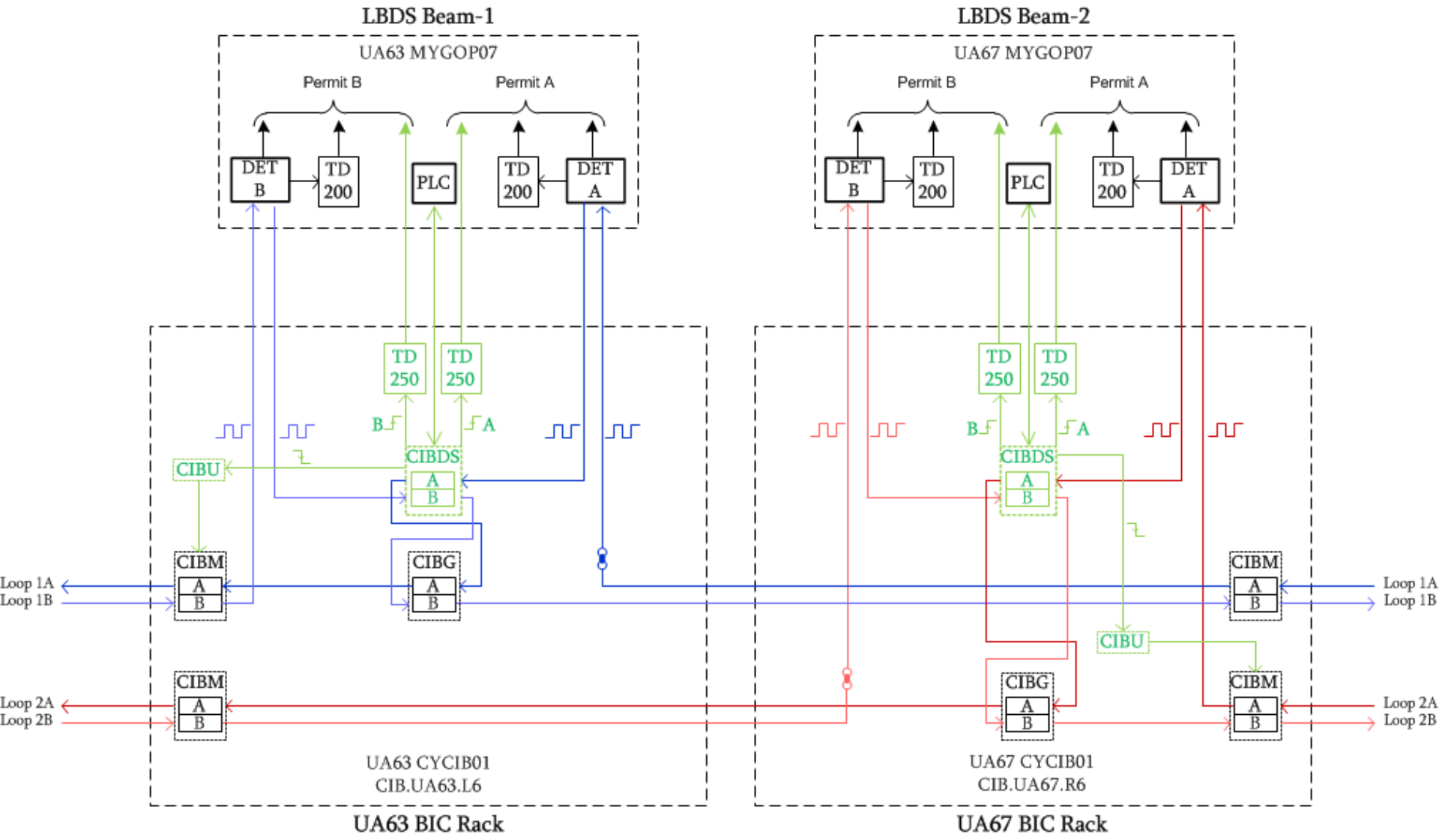
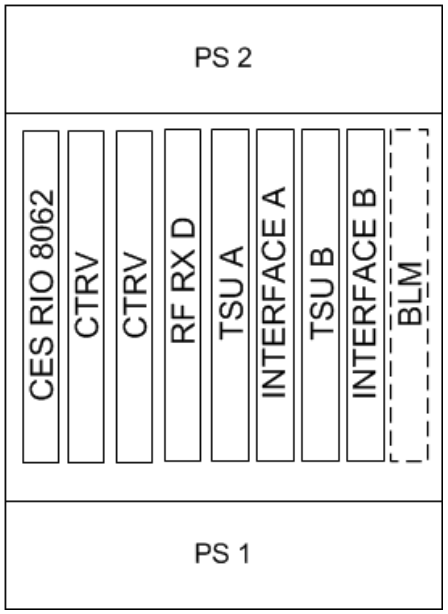
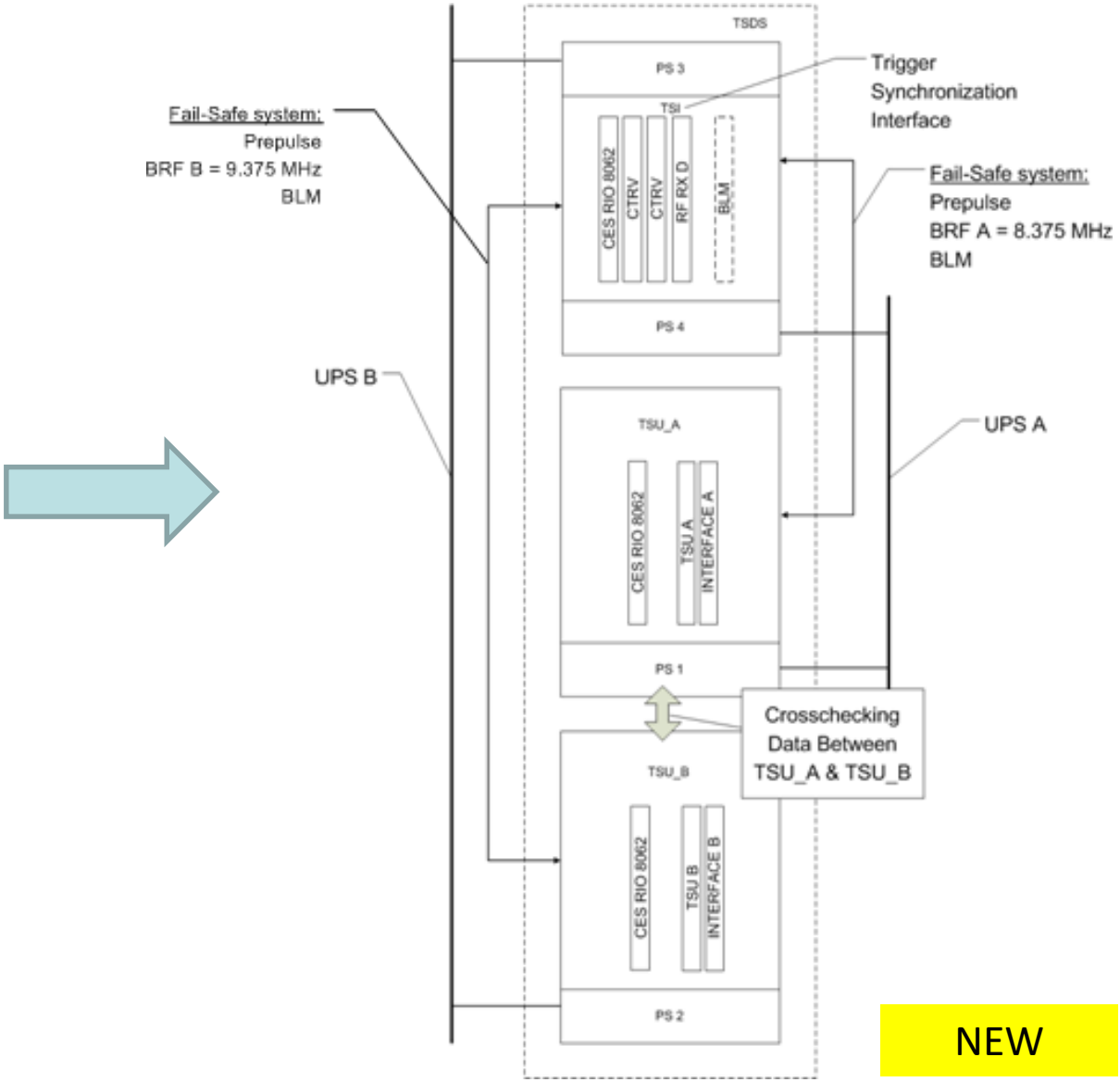


Questions


PS 2
CES RIO 8062
CTRV
CTRV
RF RX D
TSU A
INTERFACE A
TSU B
INTERFACE B
BLM
PS 1

OLD


TSDS
PS 3
TSI
CES RIO 8062
CTRV
CTRV
RF RX D
BLM
PS 4
TSU_A
CES RIO 8062
TSU A
INTERFACE A
PS 1
TSU_B
CES RIO 8062
TSU B
INTERFACE B
PS 2
Fail-Safe system:
Prepulse
BRF B = 9.375 MHz
BLM
Trigger
Synchronization
Interface
Fail-Safe system:
Prepulse
BRF A = 8.375 MHz
BLM
UPS B
UPS A
Crosschecking
Data Between
TSU_A & TSU_B

NEW