TWEPP 2022 - Topical Workshop on Electronics for Particle Physics

Tuesday 20 September 2022 – Bergen, Norway

Performance characterization and radiation tolerance evaluation of the SSA2 ASIC

The strip sensor readout ASIC of the CMS outer tracker at the HL-LHC

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On behalf of the CMS OT ASIC working group

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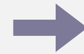
Requirements for the high luminosity tracker upgrade

Phase-II upgrade tracker requirements:

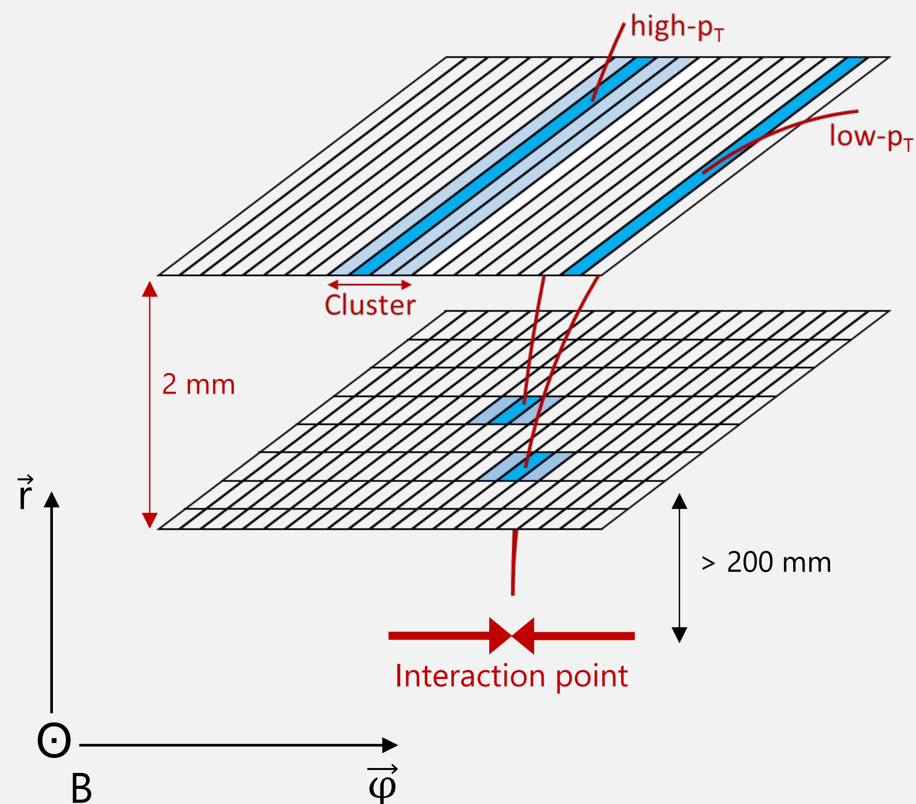
- Higher luminosity
- From 20 to 200 pileup events per BX
- Increase radiation tolerance
- Reduced material budget
- Participate in the L1 trigger
- Improve trigger performance

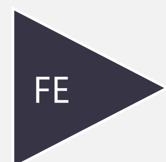


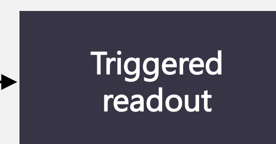
Tracker module electronics requirements:

- Increase granularity
- Introduction of a pixelated sensors
- Radiation tolerance up to 100 Mrad
- Quick and on-chip particle discrimination
- Higher trigger rate (1MHz) and longer latency (12.5 µs)
- Power density < 100 mW/cm^2
- Add tracking information to the Level-1 trigger decision

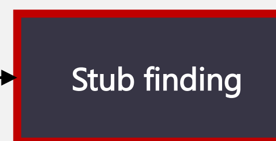
An intelligent particle tracking system based on p_T discrimination



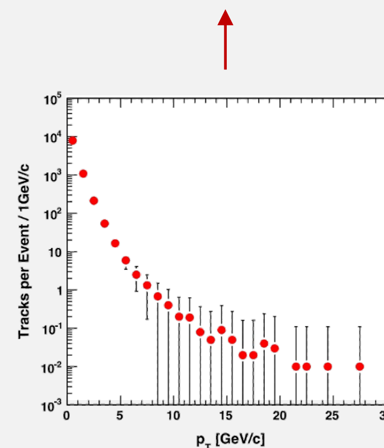




Full raw event at L1 rate (up to 10^6 events/s)



Real-time transmission of encoded information of high transverse momentum particles 40 MFrames per second

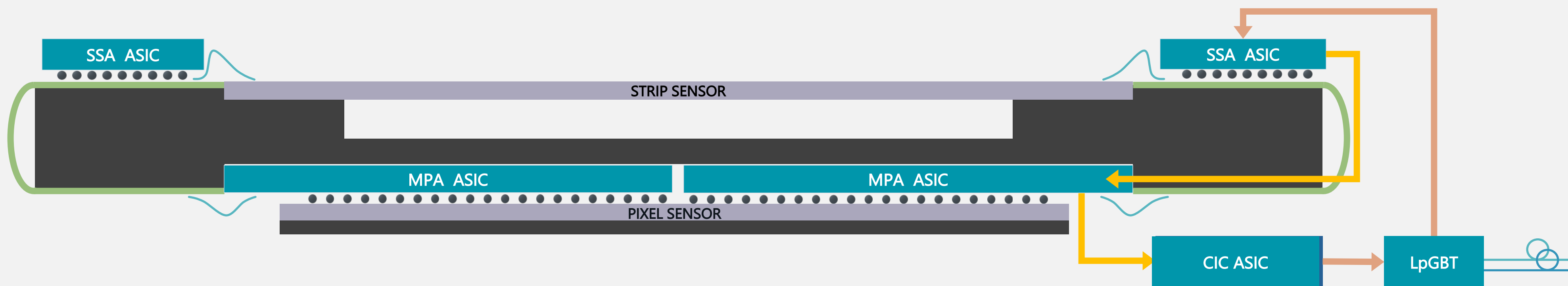


The p_T threshold should be chosen:

- High enough to reject of the background with significant data reducing factor
- Low enough to don't filter out the interesting decay products with impact in the analysis performances.

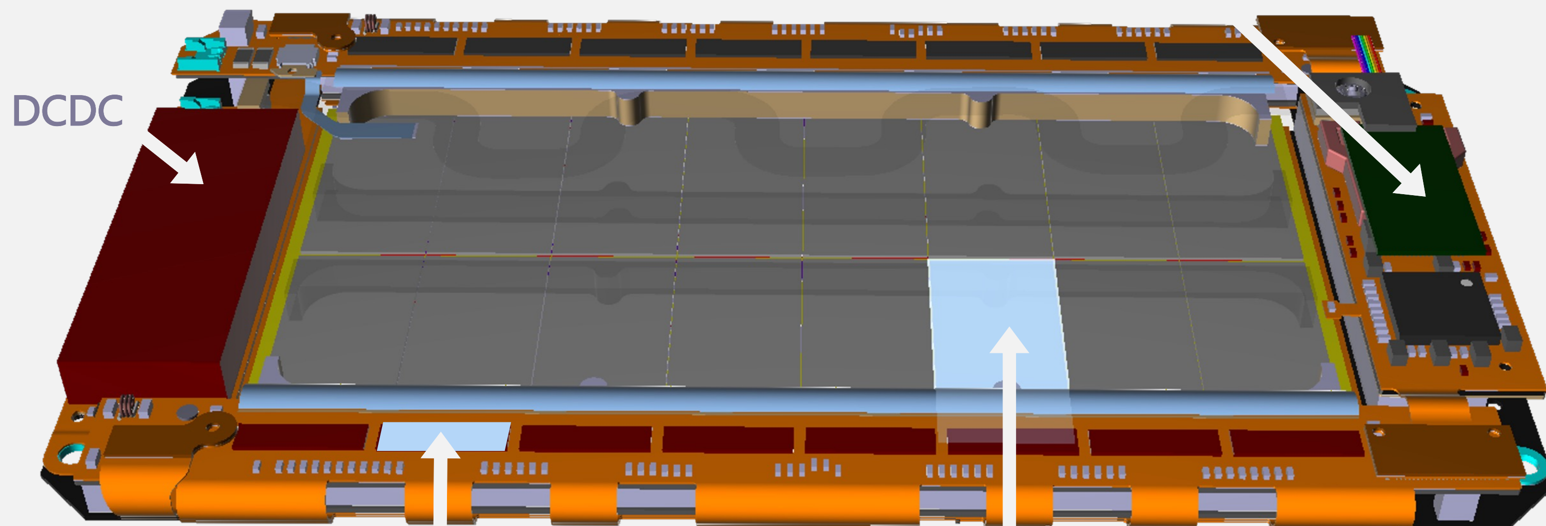
3.8T provided by the superconducting solenoid

The Pixel-Strip module



LpGBT & VTRX+

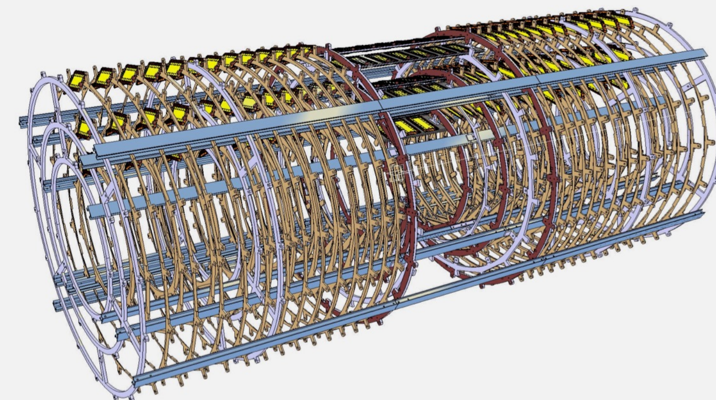
DCDC



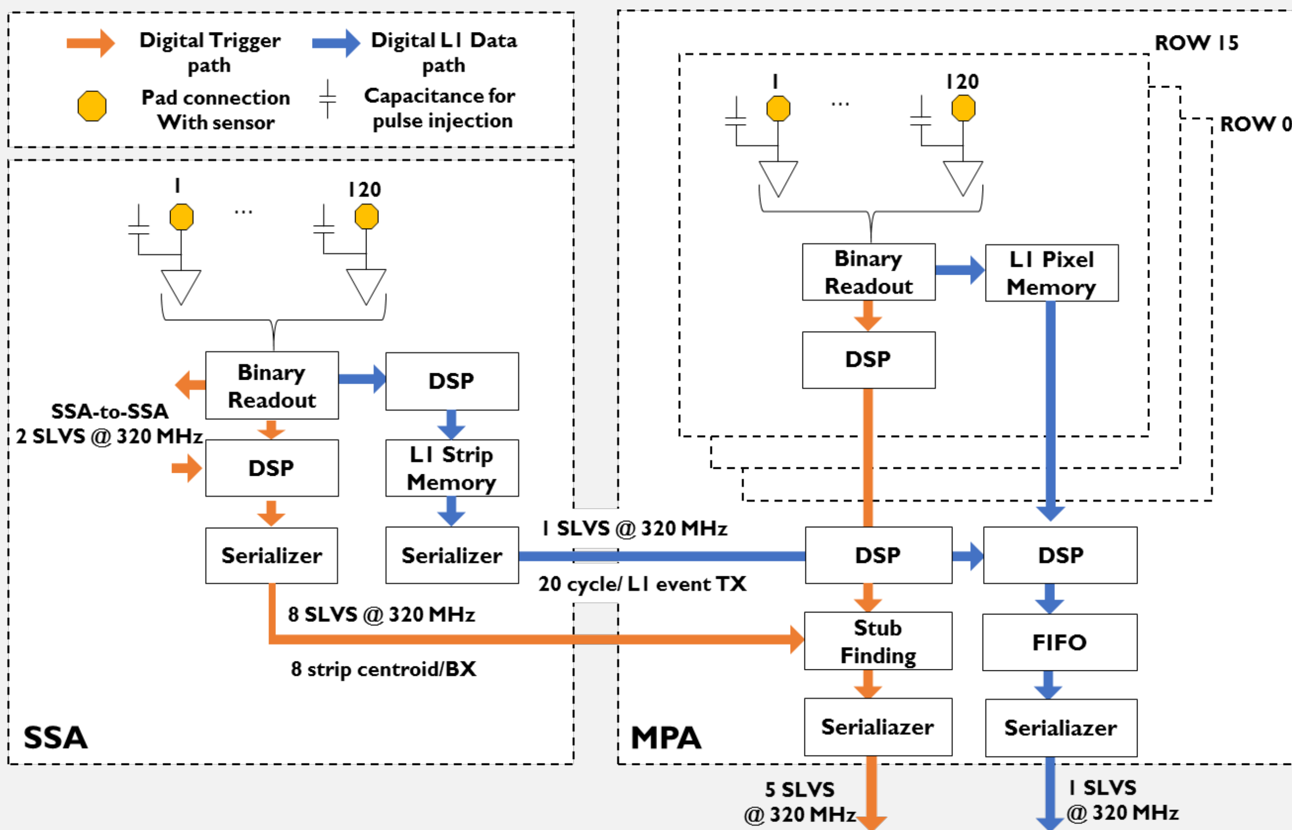
16 x SSA ASICs (Strip ROC)

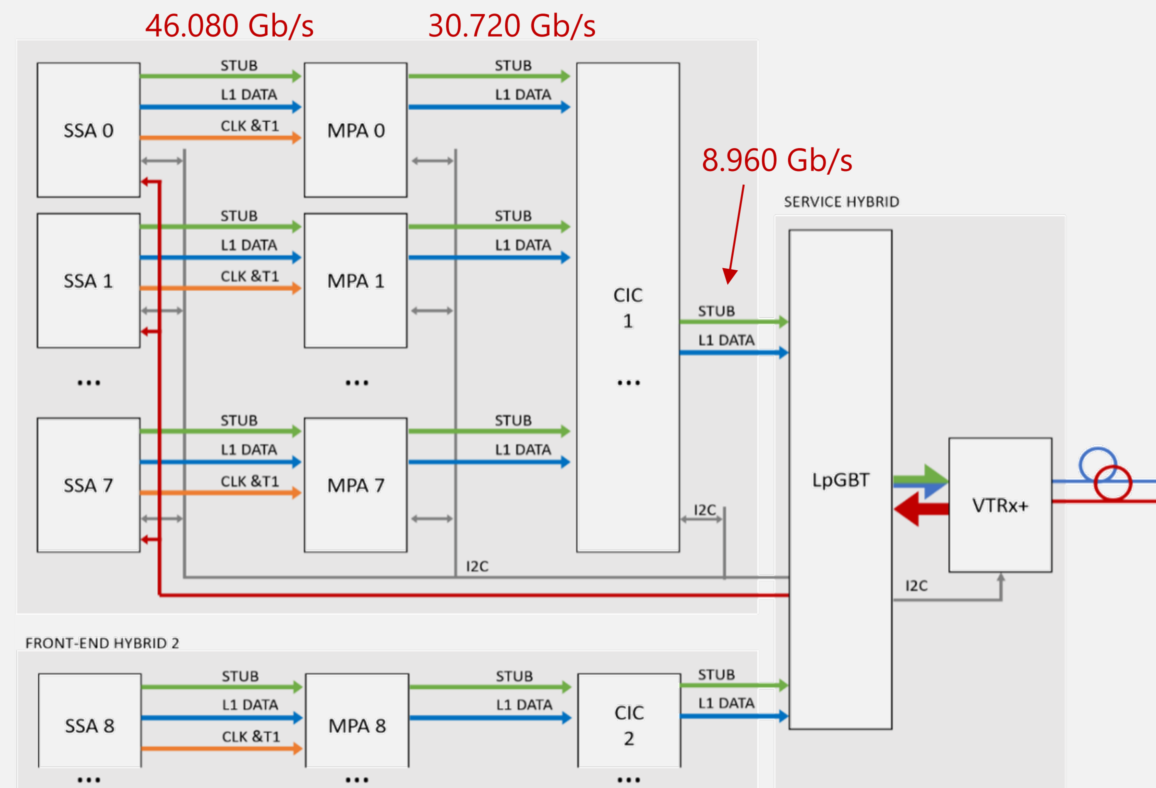
16xMPA (Pixel ROC + stub finding)

13296 Modules
44 M strip + 174 M pixels
200 m^2 of Silicon Area



System architecture and SSA block diagram

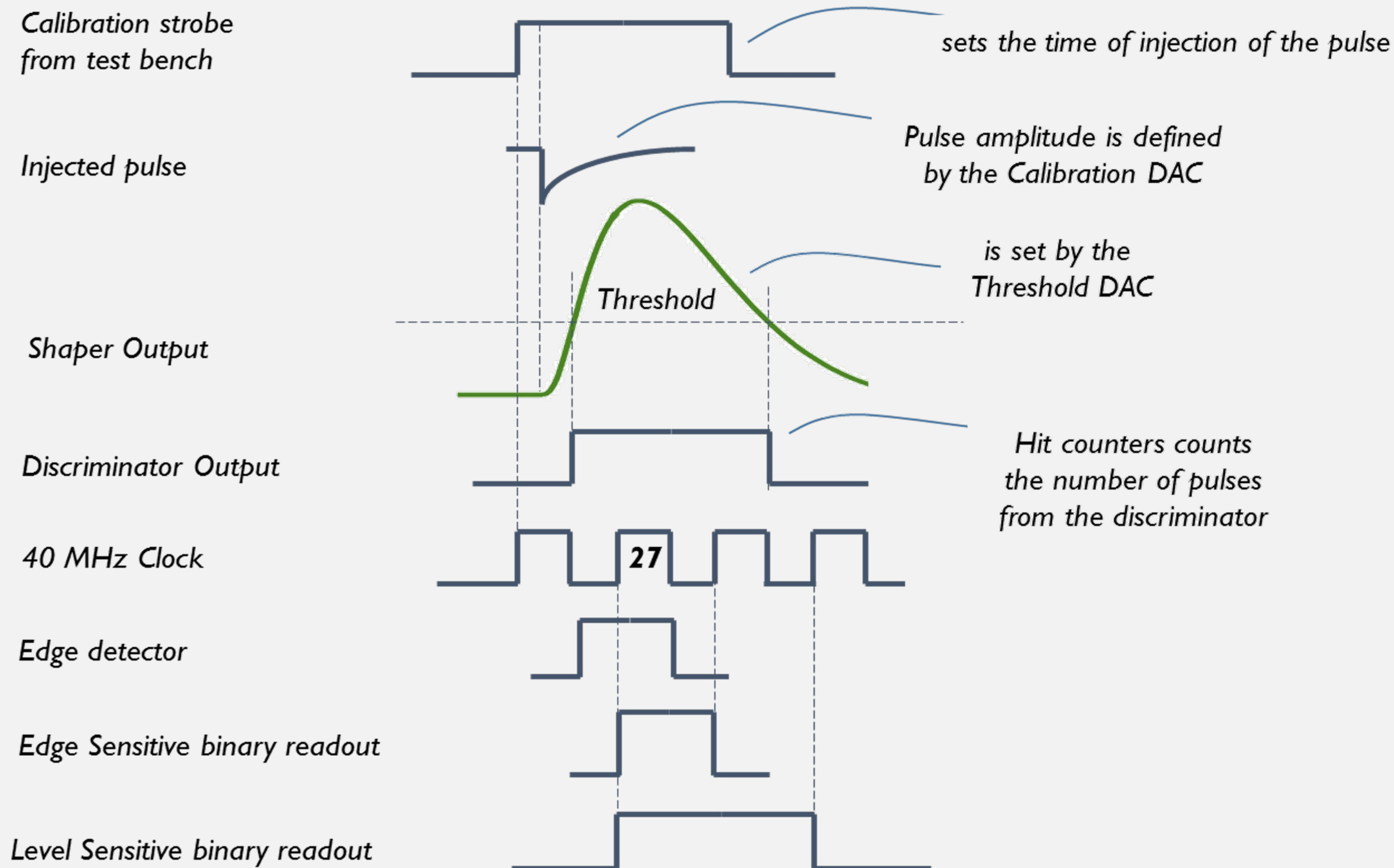




40 MHz rate for high-pT particles
1.6 Gb/s
very low latency: < 500 ns

Full frame at L1 trigger rate (1MHz)
320 Mb/s

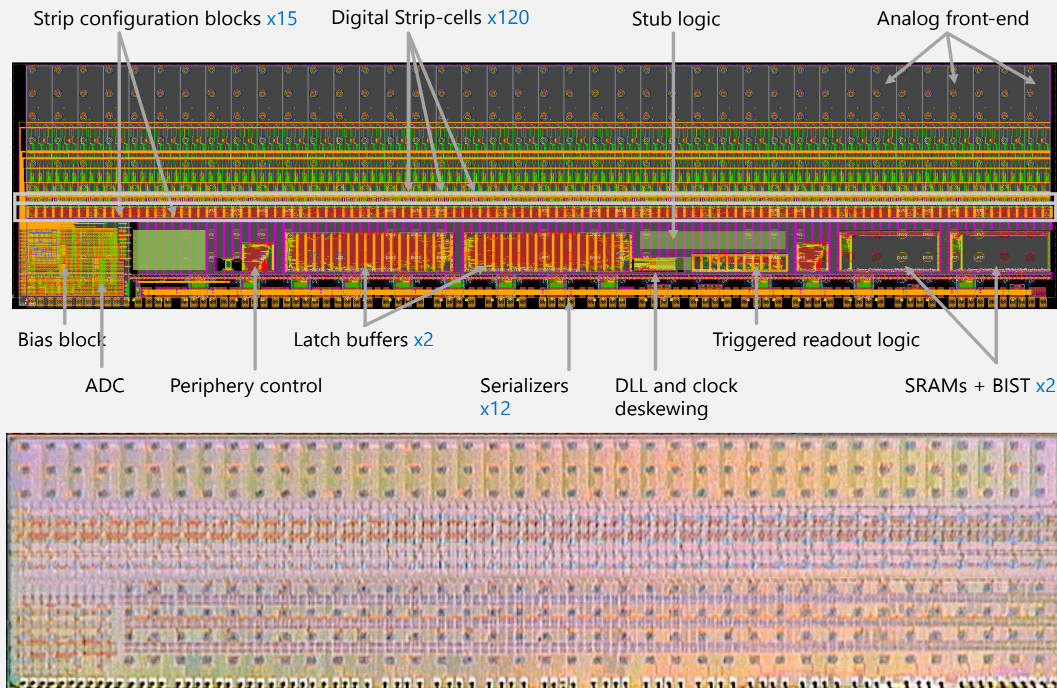
The SSA front-end characterization

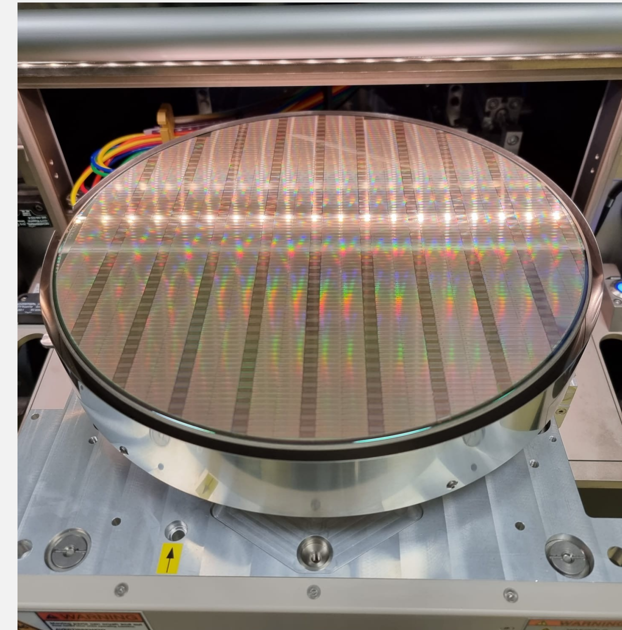


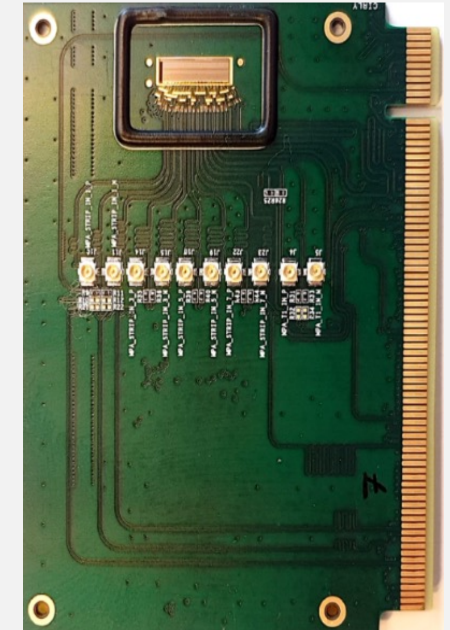
- Double threshold binary readout Detection hit threshold + High ionizing particle
- Trimming DAC per channel for threshold equalization
- Average occupancy > $2{\cdot}10^{-2}$, cluster size mean = 2 → no dead-time between events
- Multiple readout modes
- Controllable sampling clock phase with 2-stage clock deskewing (DLL)
- Front-end characterization can be carried out thanks to the internal test features and calibration system

The SSA2 ASIC

- The final version of the SSA ASIC was summitted for a **full mask-set engineering run** in 2021
- The first wafer was thinned, bumped and diced allowing for characterization and radiation tests on carrier board
- A dedicated test system and analysis software was developed







Main functional tests

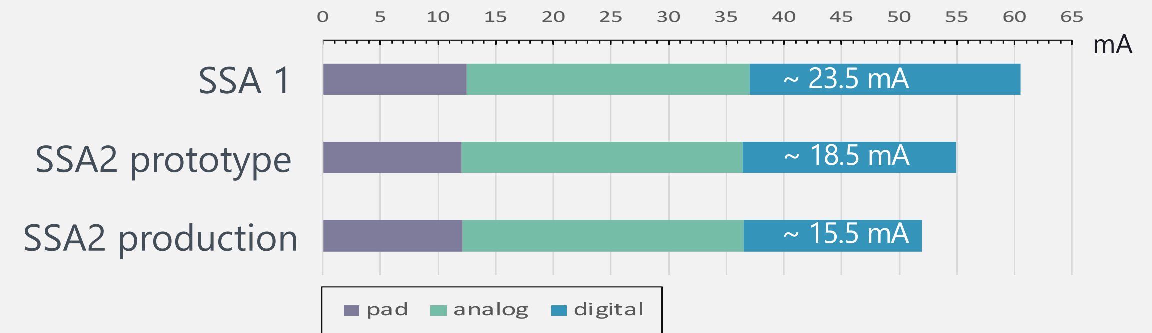
Summary of functional tests :

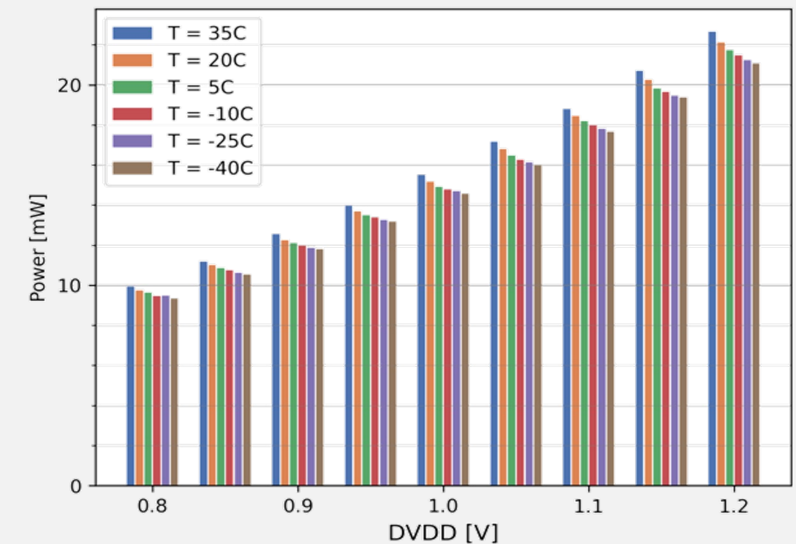
- Reset behaviour and ASIC Initialization
- Configuration and slow-control operations
- Bias measurements and DACs linearity
- ADC and temperature sensor
- S-Curves and threshold trimming
- FE noise measurements
- Lateral transmission
- STUB DATA and clustering (0.9V to 1.1V)
- L1 DATA and HIP FLAGS (0.9V to 1.1V)
- SRAM and LATCH memories
- Ring oscillators
- E-Fuses burning
- DLL measurements
- Scan-chain functionality

And others ..

	Chip 1	
DVDD	Stub	L1
1.25 V		
1.20 V		
1.15 V		
1.10 V		
1.05 V		
1.00 V		
0.95V		
0.90 V		
0.85 V		
0.80 V		
0.75 V		

Power consumption

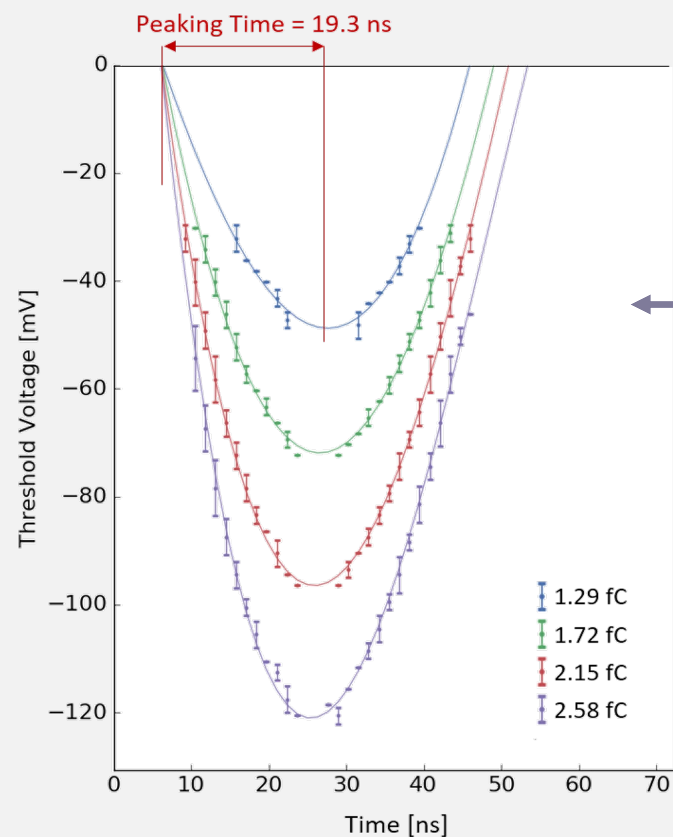




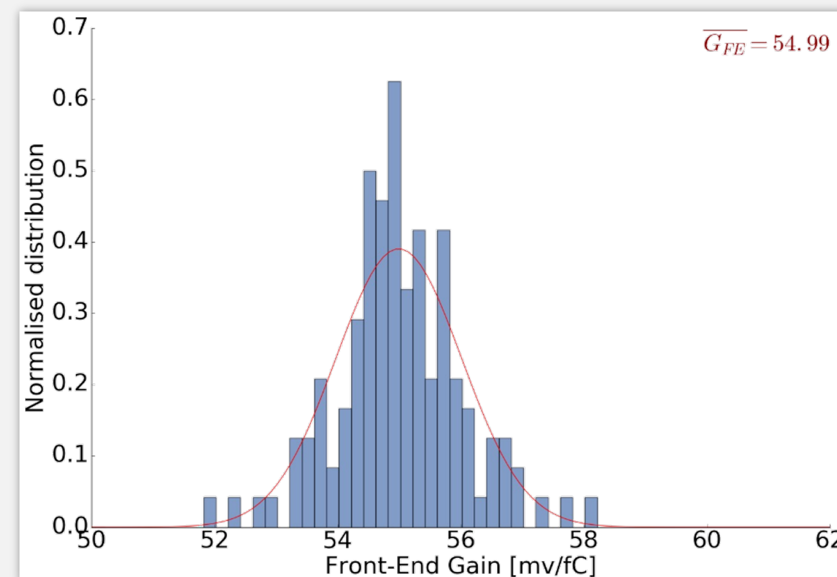
The SSA front-end characterization

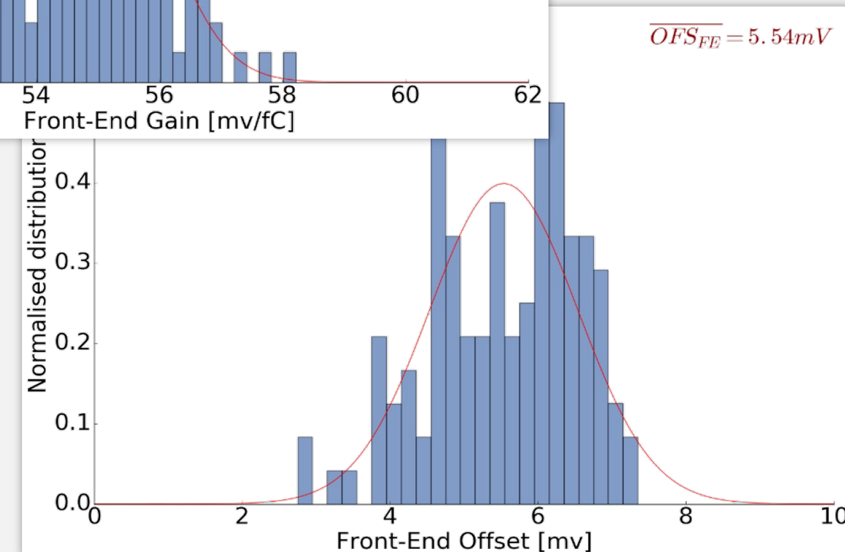
Shaper pulse reconstruction

by injecting a known charge via the SSA calibration system and acting on threshold, calibration pulse delay-line and clock deskewing DLL.



Peaking time < 25ns with linear behavior and up to 8fC



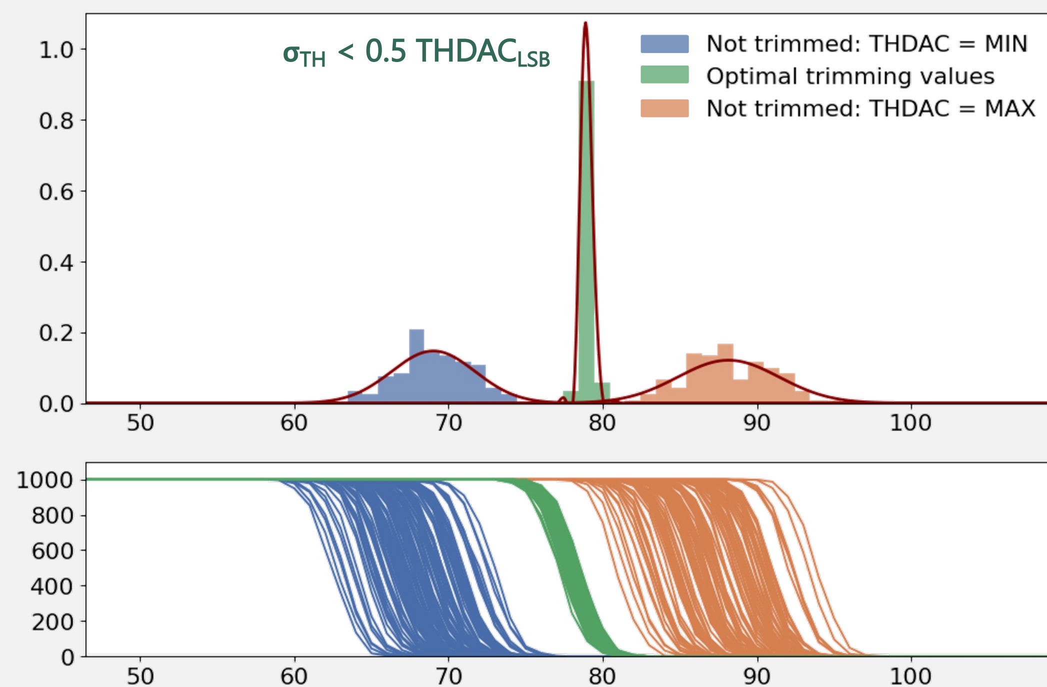


Gain and offset distributions

for a non-trimmed SSA ASIC

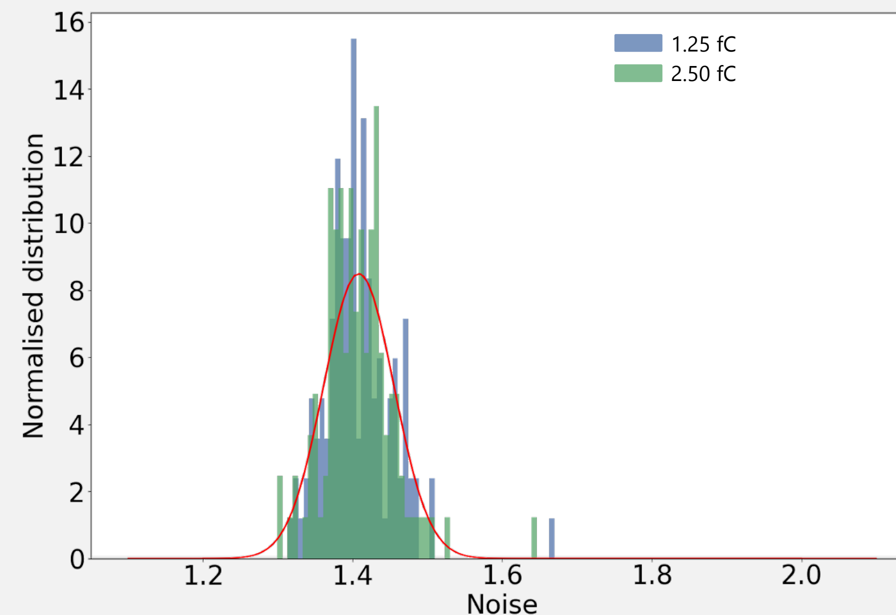
Front-end characterization

Threshold trimming



Trimming performed at 2.0 fC.
Threshold spread evaluate for 2.0 fC and 1.25fC

Front-end noise measurements

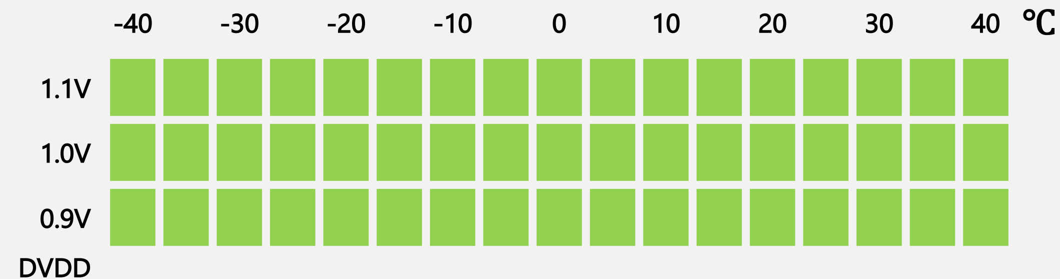


Channel input noise evaluated as the standard deviation of the error function fitting the S-Curves (1.25 fC and 2.0 fC)

SSA temperature tests

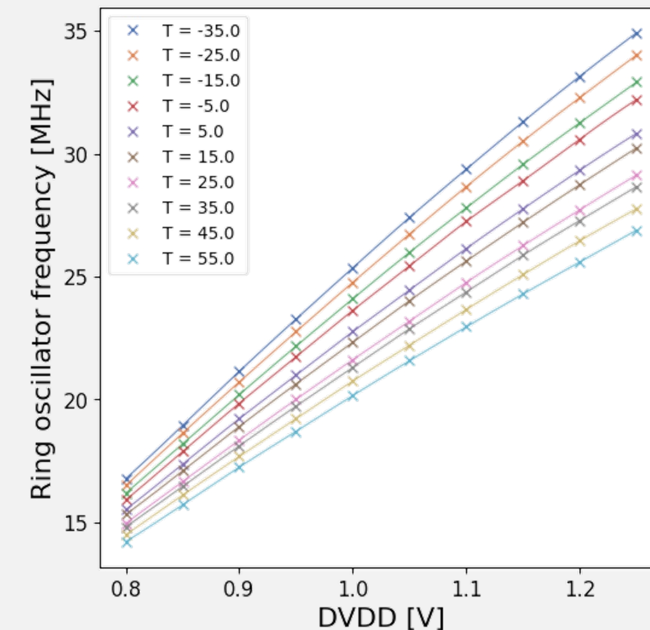
Temperature Characterization summary

- No errors or timing issues observed on digital logic



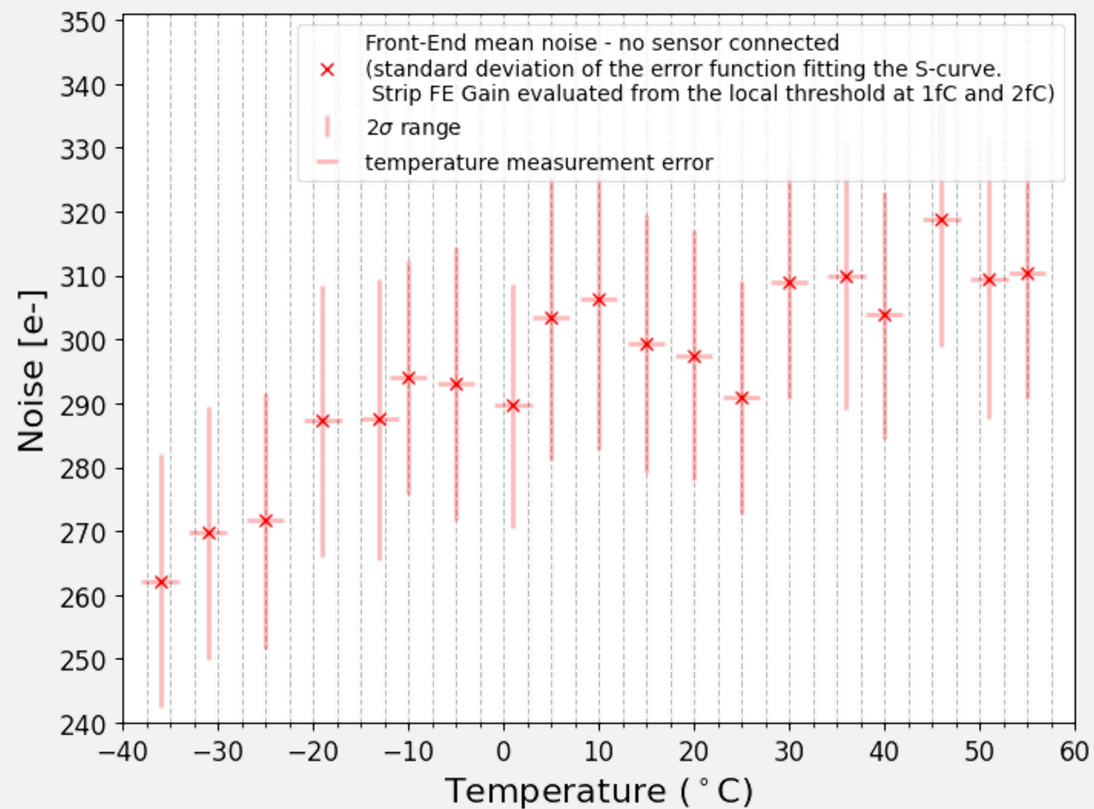
- No errors or issues observed in analog FE
- Bias structures variation within compensating range
- FE noise change within expectation

- Full set of digital functionalities tests
- Tests of memories (with BIST) and configuration
- Characterization of all bias parameters
- S-Curve for FE Gain, Noise and Trimming
- ADC, E-Fuses, Voltage swipes and several others

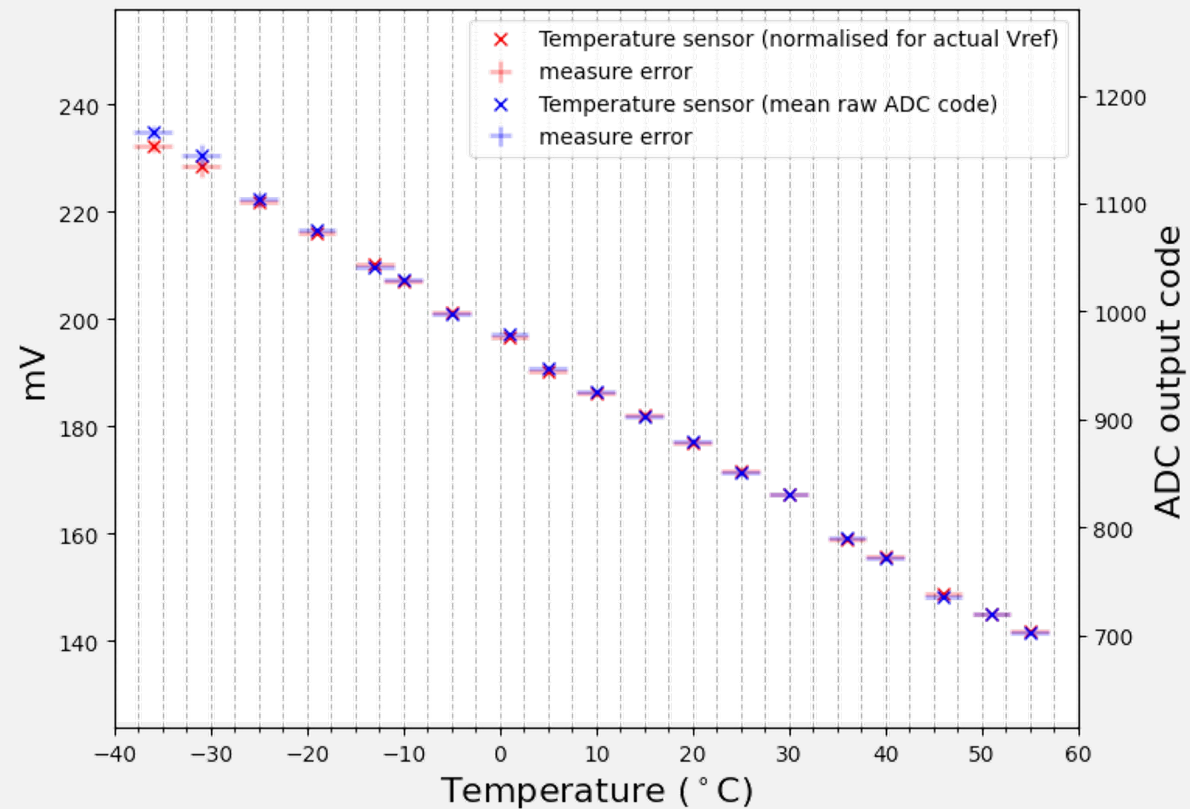


Temperature measurements

Analog Front-End Noise vs Temperature

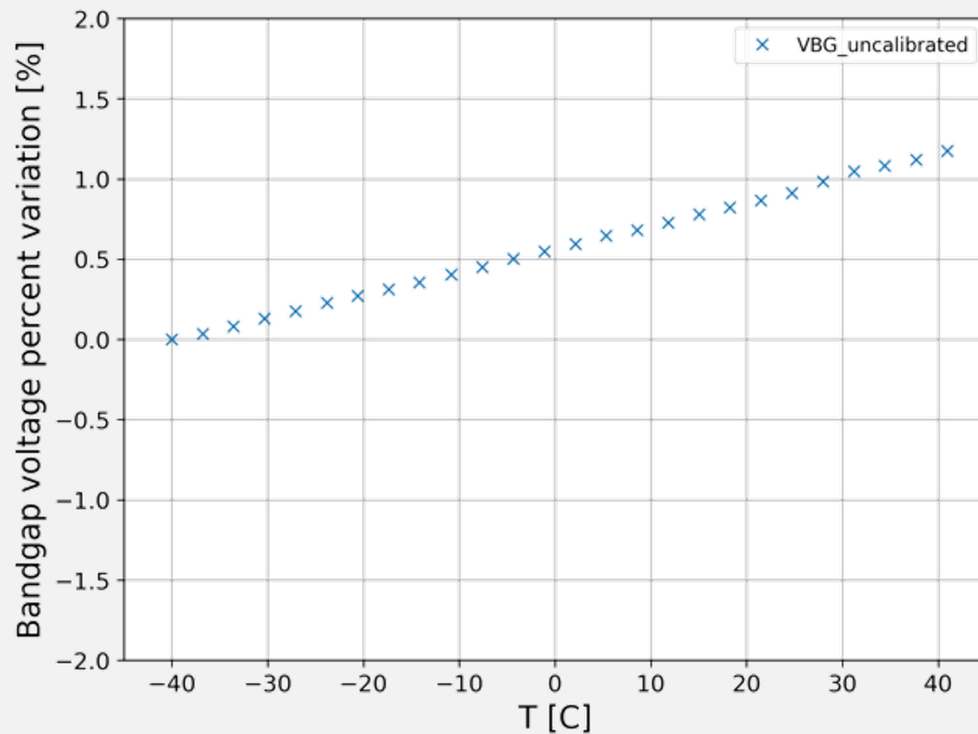


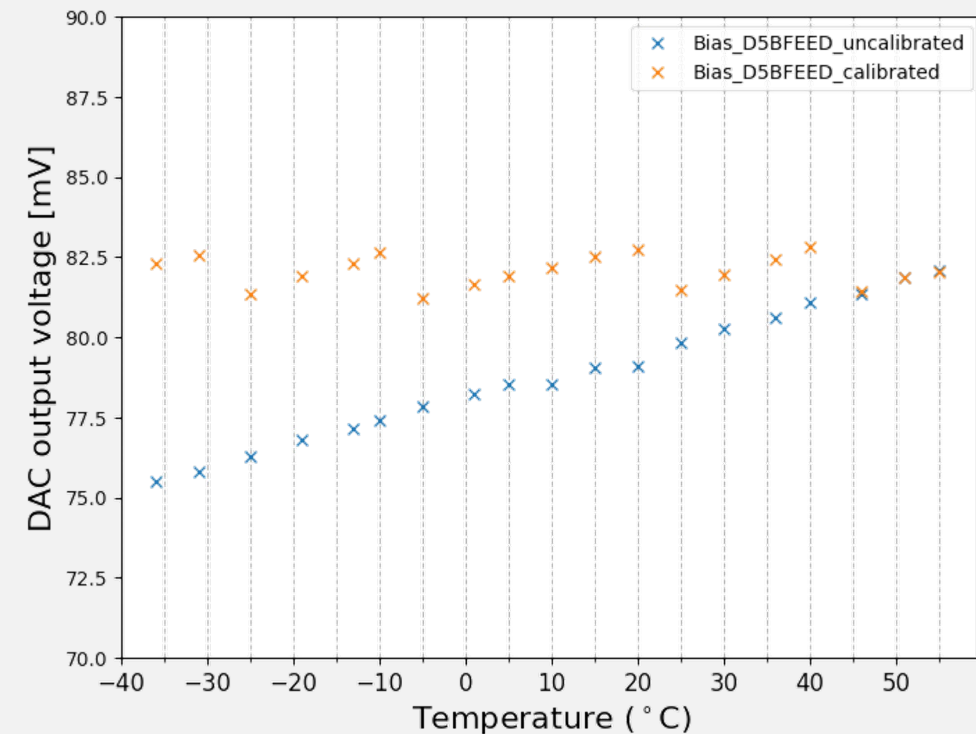
SSA Embedded temperature sensor measure



Temperature measurements – Bias Calibration

- The SSA include several 5-bit DACs in the bias structure to provide stable front-end performances
- The measurements confirm that all parameters variation can be compensated by the internal calibration system

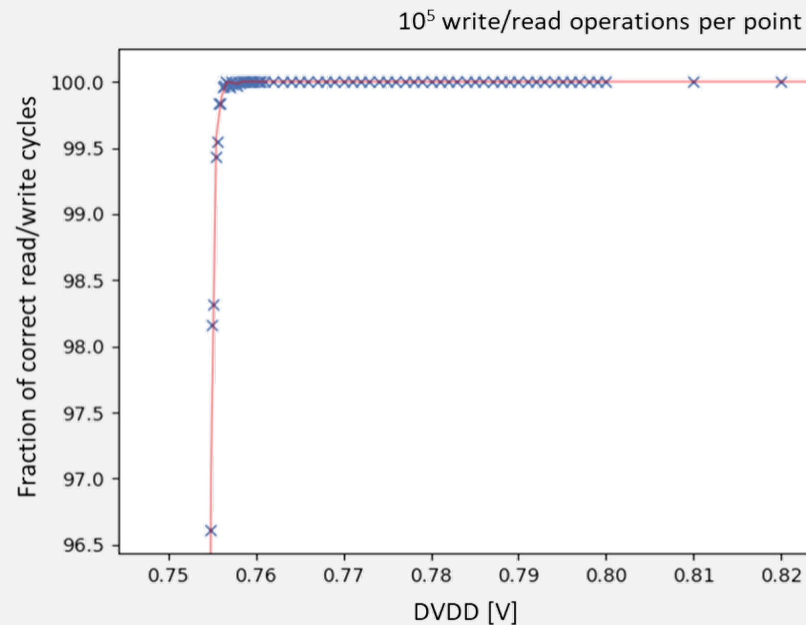




Design for Testability

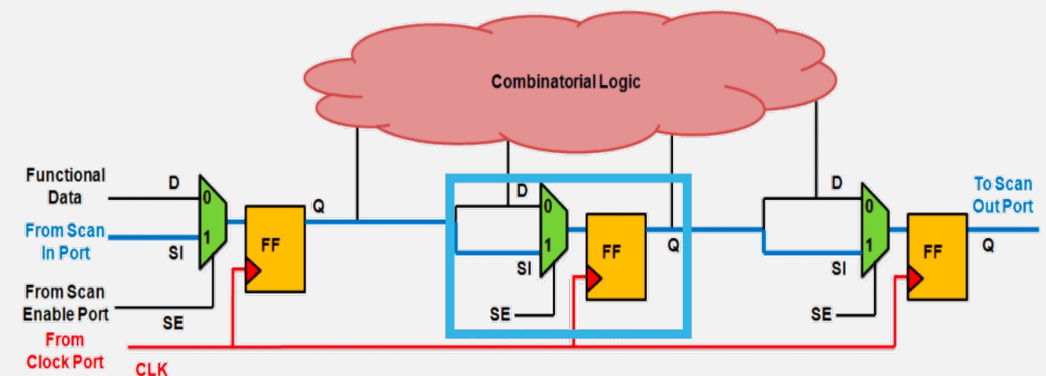
Memory Built-In-Self-Test

- Test full memory functionality in <1 ms
- Results saved in internal registers accessible via slow-control
- Clock gating during normal operation (only leakage power)



Scan Chain

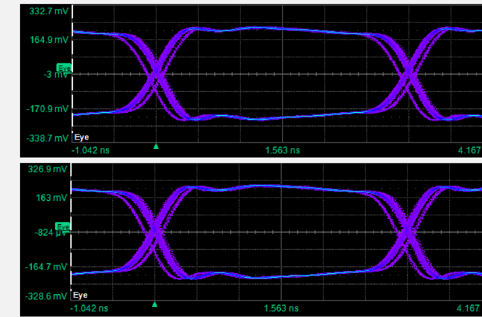
- 92% of fault coverage in SSA ASIC
- Custom approach for triplicated design
- SHIFT, RESET and CAPTURE tests
- A total of ~950 test vectors required
- Full test duration < 300 ms
- Scan-chain in SSA operates correctly up to 20MHz

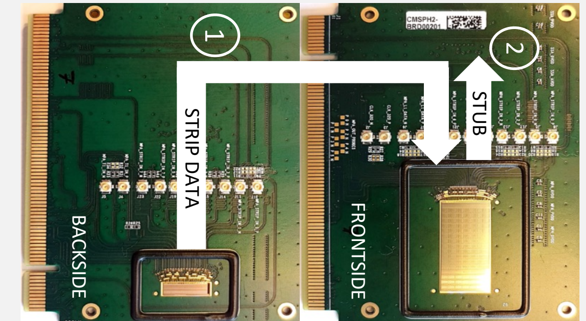


Communication tests

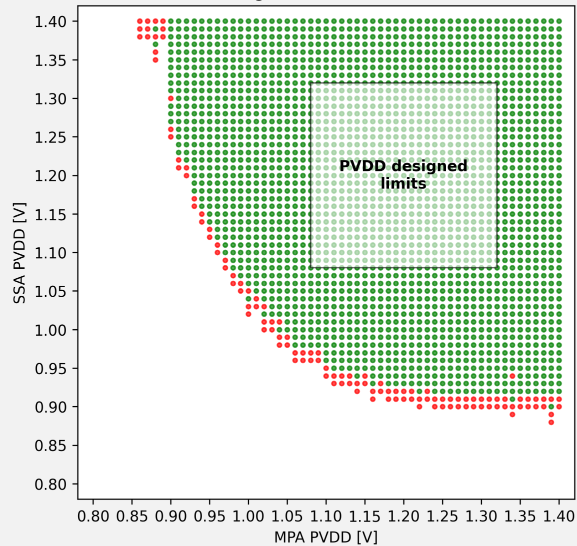
SSA → MPA Communication

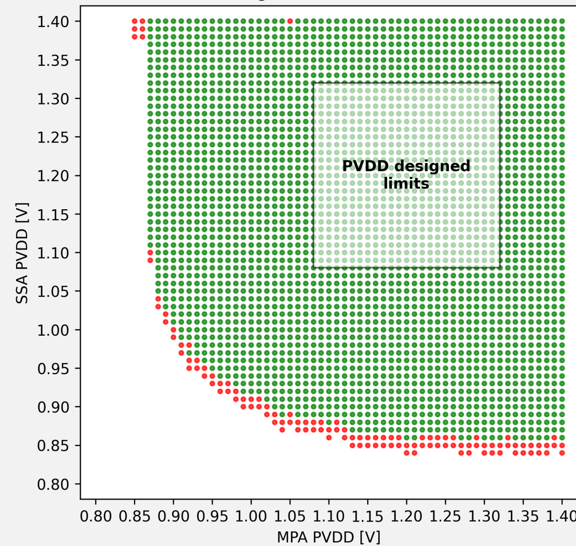
- No phase aligner at MPA input due to power restrictions
- The communication rely on precise design of the timing
- SSA-MPA communication timing was verified in static timing analysis and simulated post-layout in all cross-corner combinations (UVM verification environment)



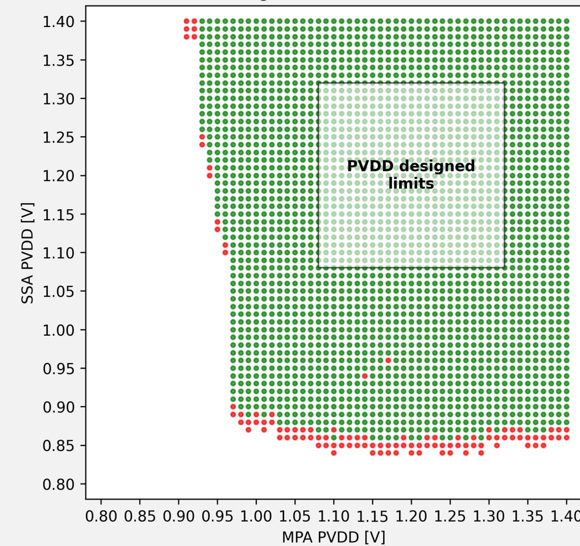


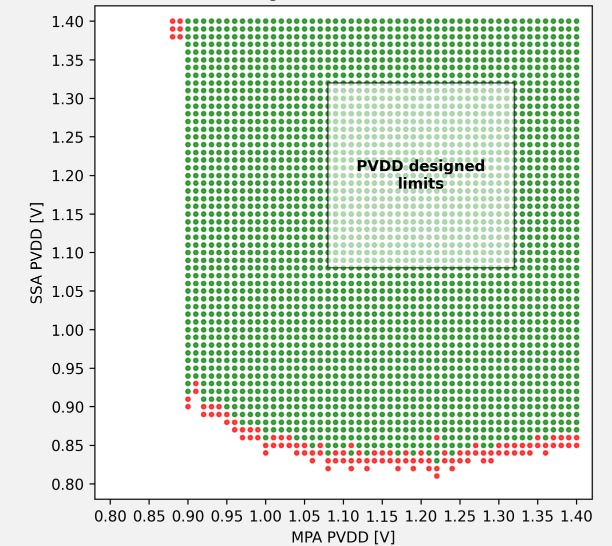
−35°C





+35°C

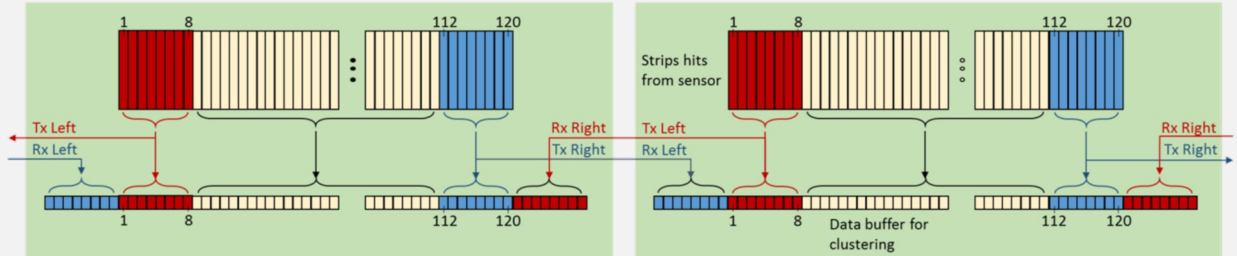




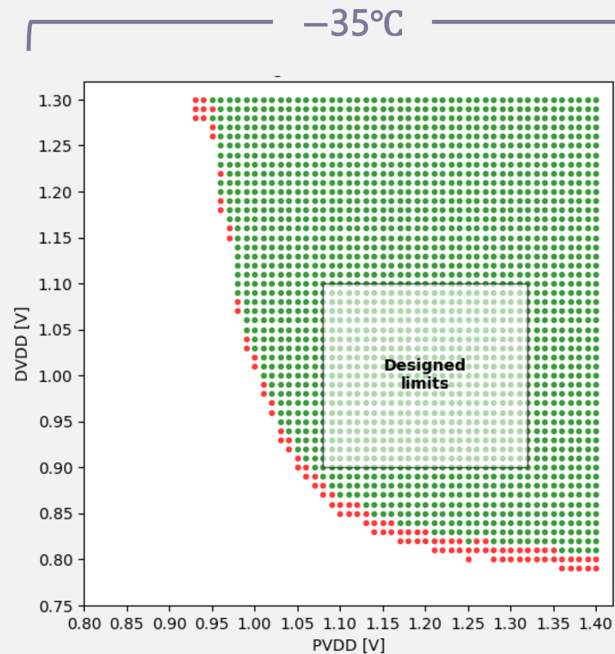
Communication tests

SSA → SSA Communication

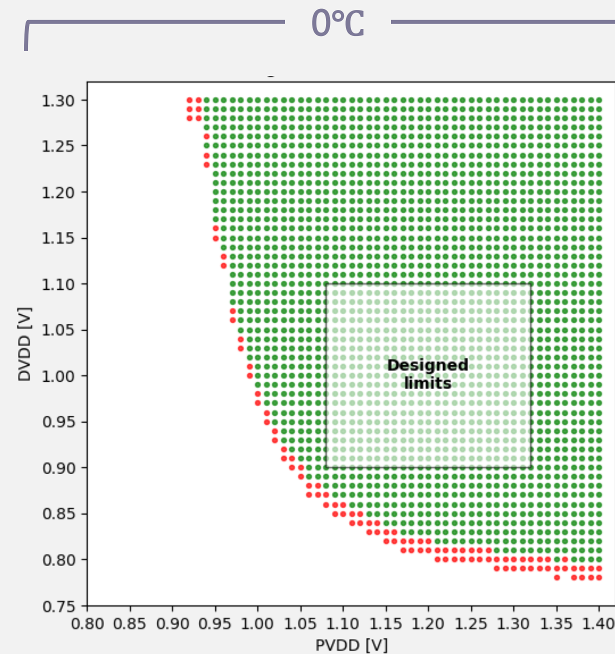
- Lateral communication for clustering among SSA
- Improve stub efficiency of ~2%
- No phase aligner possible. The communication rely on precise design of the timing for all corners



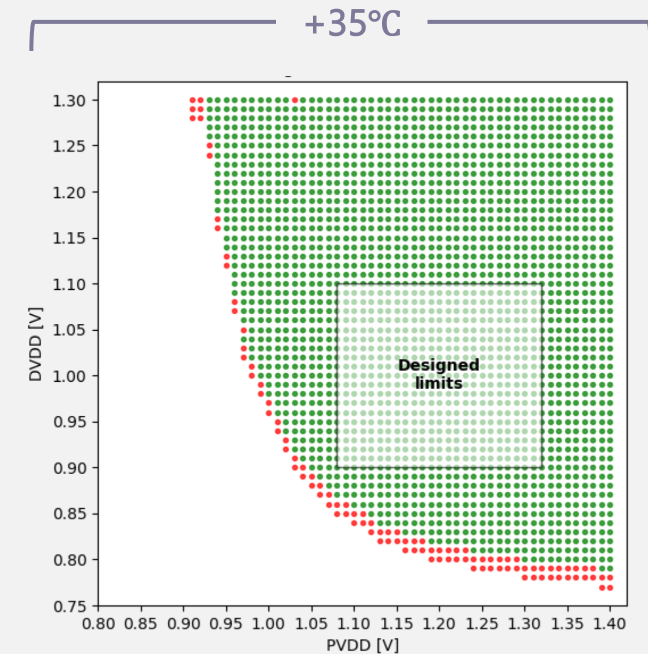
−35°C



0°C



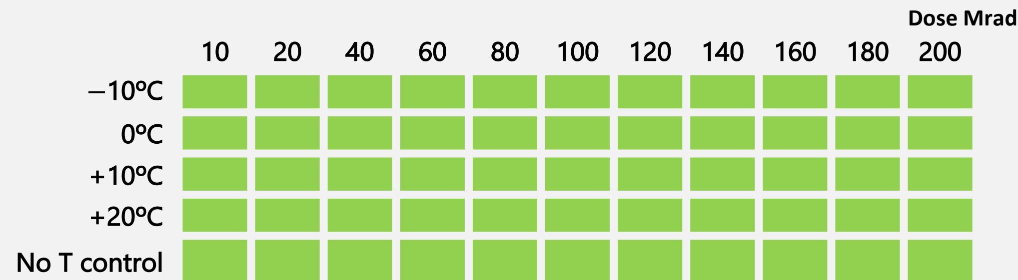
+35°C



SSA new Total Ionizing Dose characterization

X-ray TID Characterization summary

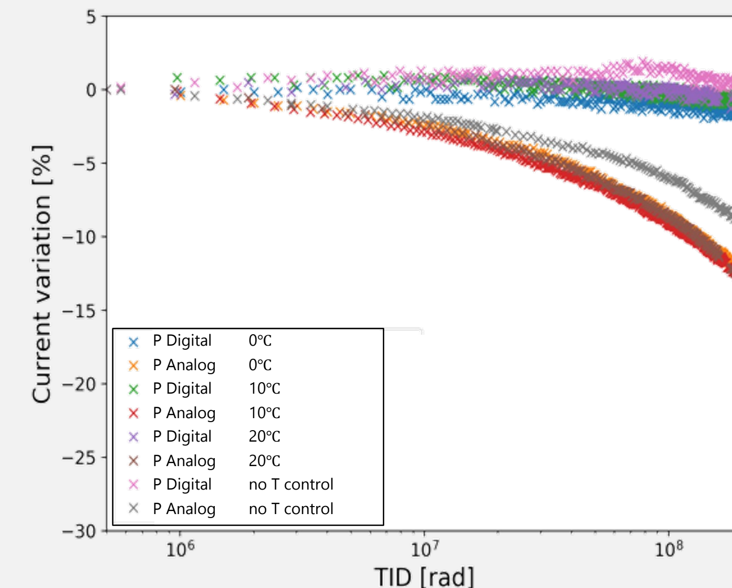
- 4 chips have been irradiated up to 200 Mrad and 1 chip up to 350 Mrad
- No errors or timing issues observed on digital logic



- Bias structures variation within compensating range
- FE noise change within expectation
- ADC reference voltage variation larger then expected:
  - Received PCM data from the foundry
  - Needed changing the target reference voltage to keep stable the DAC output up to 250Mrad.

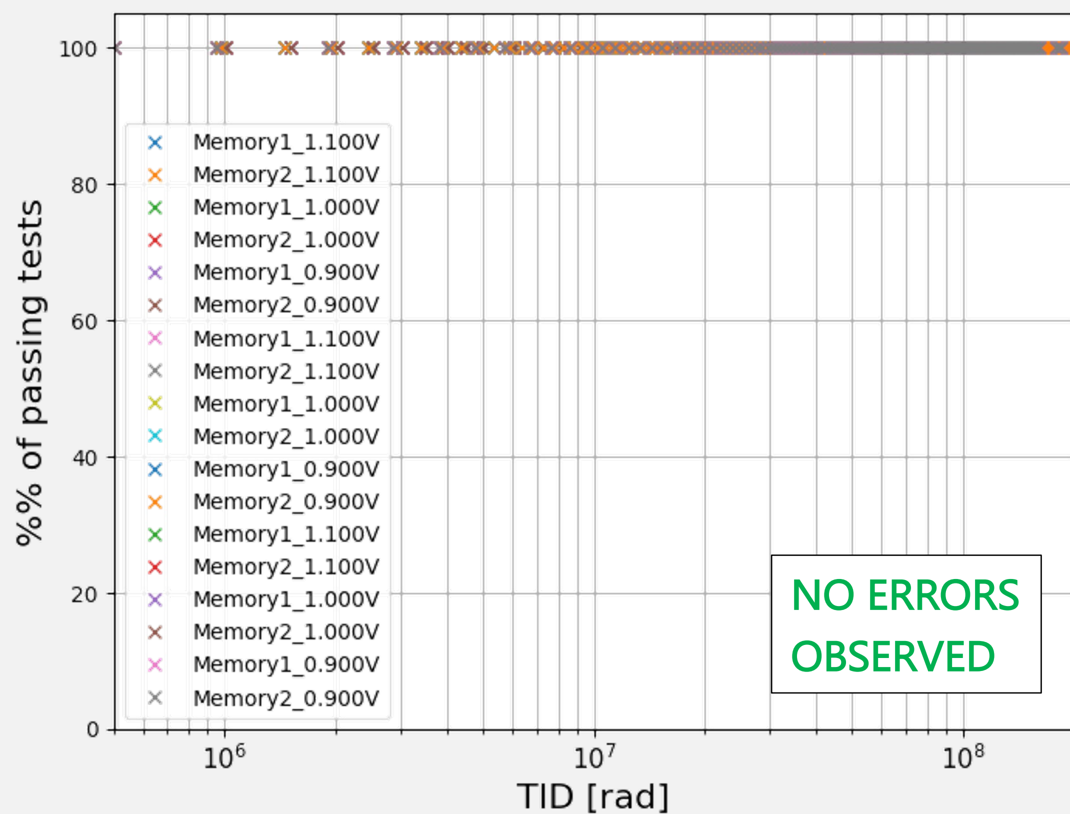
TID Test routine:

- Full set of digital functionalities tests
- Tests of memories (with BIST) and configuration
- Characterization of all bias parameters
- S-Curve for FE Gain, Noise and Trimming
- ADC, E-Fuses, Voltage swipes and several others

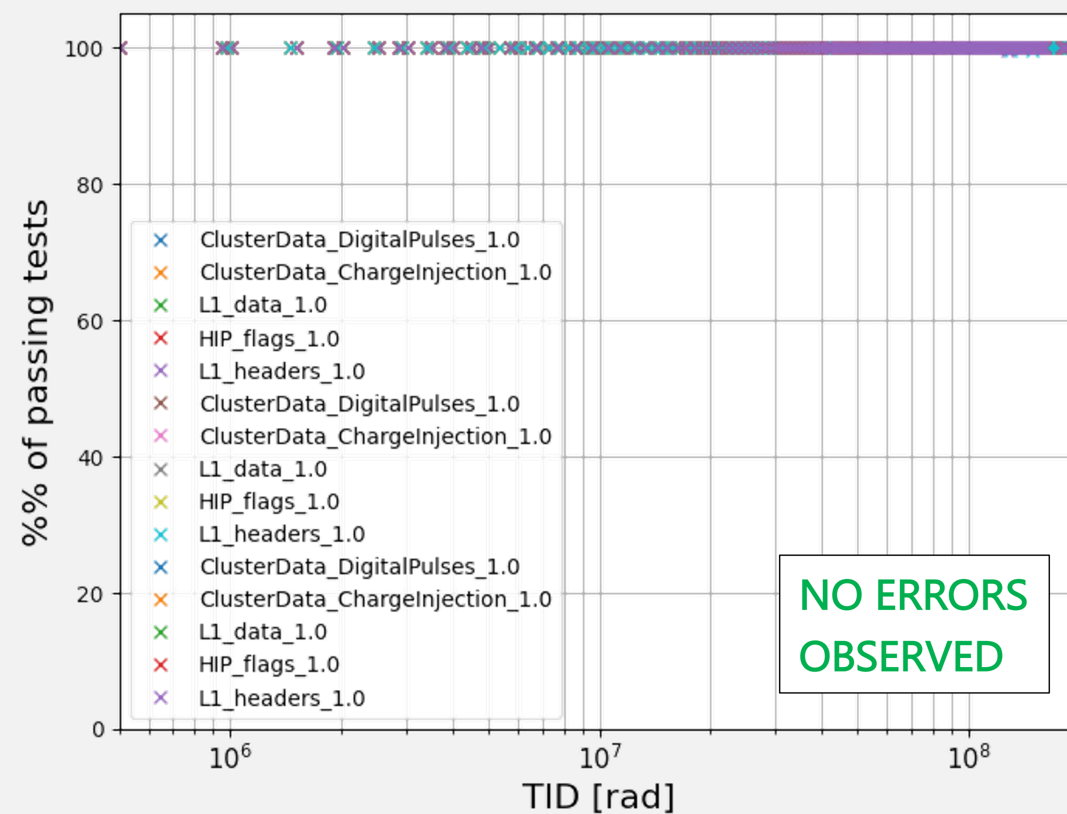


Total Ionizing Dose characterization

Memory test with Built-in Self Test (BIST)

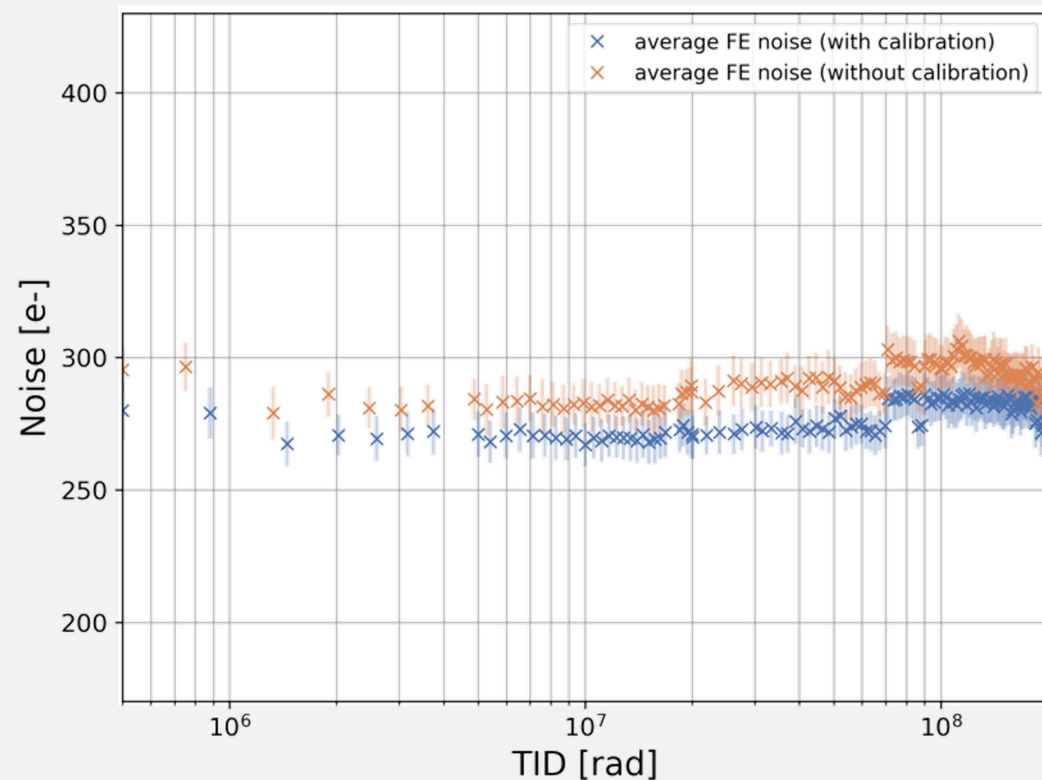


Digital functionalities tests

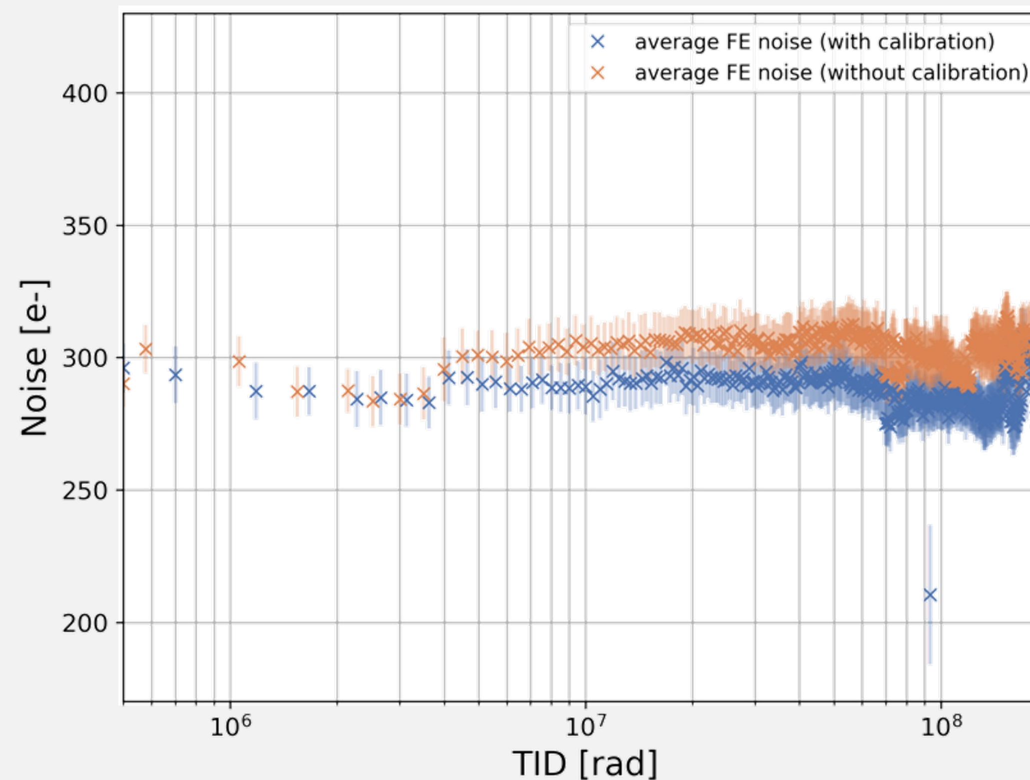


SSA Front-End equivalent noise evolution with TID and temperature

SSA 2.1 average FE noise* vs TID at -10°C



SSA 2.1 average FE noise* vs TID at +20°C



* FE noise evaluated on the S-Curves – 2 fC internal charge injection – Sensor inputs floating

ADC reference voltage variation with TID (5-bit DAC for corner compensation)

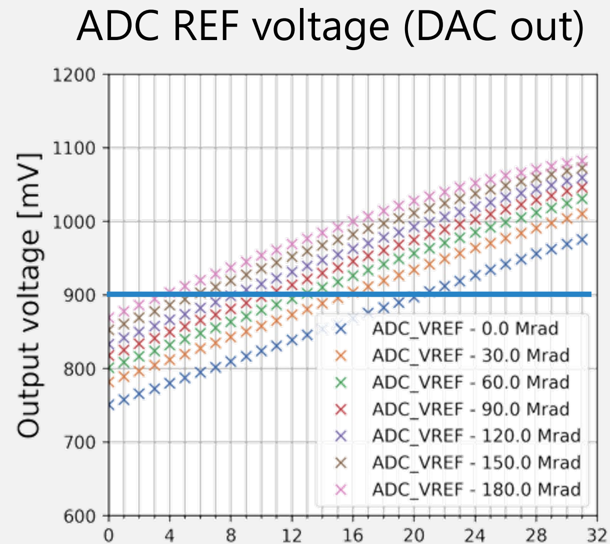
ADC REF voltage (DAC out)

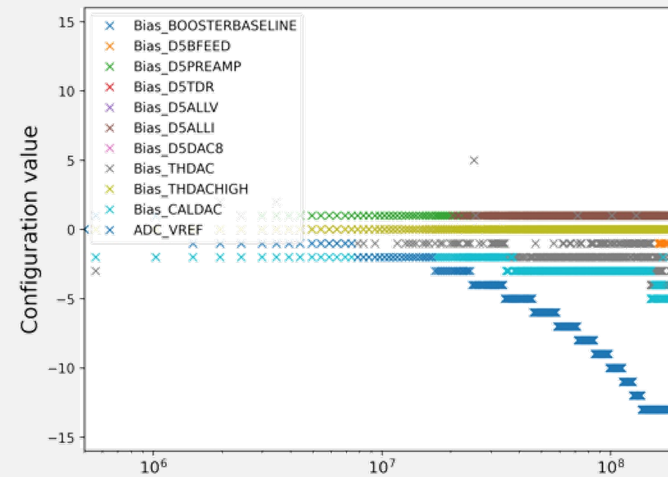
Calibration value to compensate

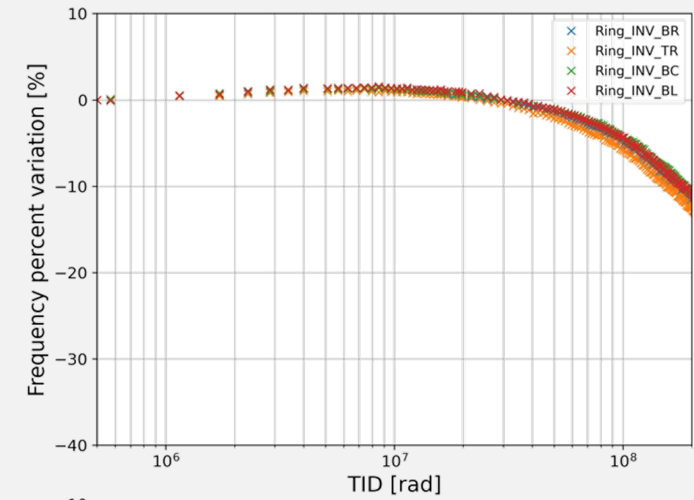
Ring oscillators

SSA2.1

Engineering run

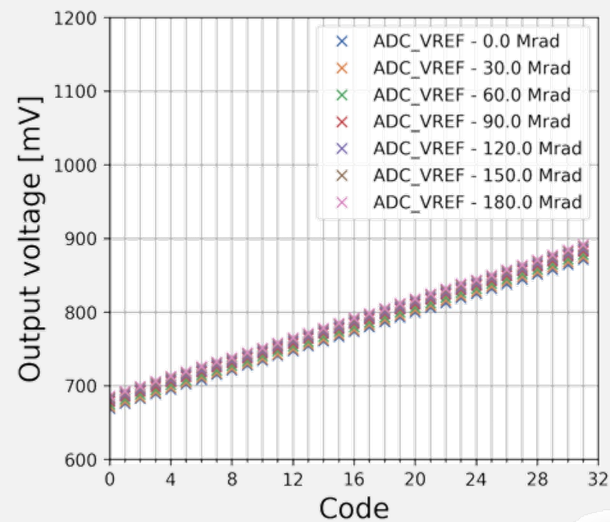


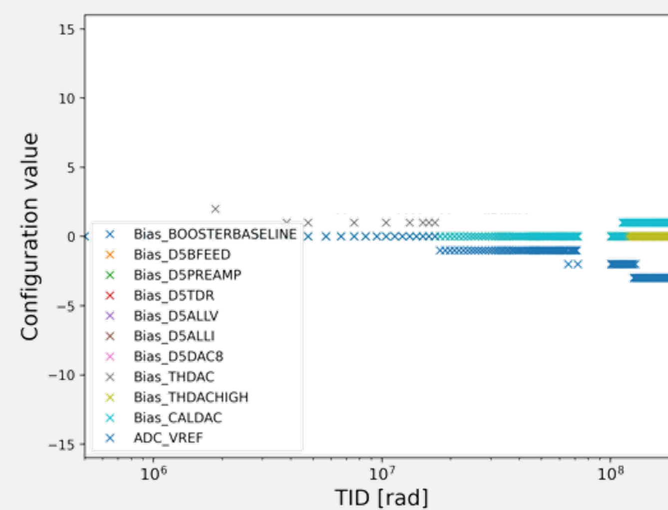


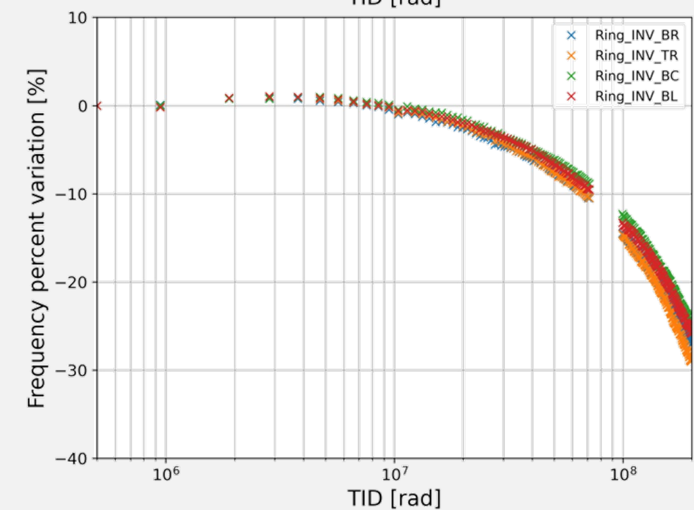


SSA2 MPW

prototype







SEE tolerance

State machines

- Triple module redundancy (FULL)
- Triplicated Clock-trees
- Triplicated Reset distribution
- FF minimum distance 15um

Latch FIFOs

- Control and header fields triplicated
- Data latches not protected

Data pipeline

- No SEU protection applied due to limited power budget

Clock tree

- Clock tree triplicated
- The non-triplicated logic uses the voted clock in critical areas
- The non-triplicated logic uses one of the branches in non-critical areas:
  - Simplify scan-chain insertion
  - Helps in reducing buffering for hold fix (power)
  - Allow for CPPR on the 3 branches

Triplicated pads for

- Clock
- Reset
- Control
- Scan-Chain IOs

Configuration registers

- Triple module redundancy with error detection and self-correction
- Clock enabled only during
  - asynchronous readout operation,
  - configuration operations
  - self-correction

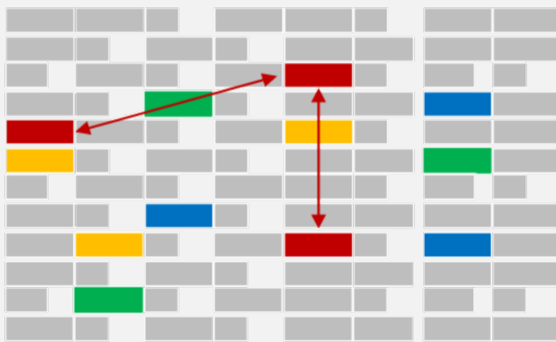
Glitch filters

- Reset inputs
- TEST-MODE signal
- Scan-chain TEST POINTS control (on the control of the system clock / test clock selection multiplexers)

SEE tolerance

Physical implementation

- Use of instance space groups among triplicated registers
- Avoid logic simplification by synthesis and P&R flow
- Spacing for clock and reset:
  - After CTS locate the critical cells and impose a minimum distance
  - procede in successive ECO placements and ECO routing steps



Functional simulation

- System Verilog UVC for randomize the injection (constrained from the specific test case)
- The randomization is constrained accordingly: Error probability, average SEE rate, minimum time split, etc..
- Injection of single event effects in multiple ASICs at the same time to evaluate the consequences that SEE in an ASIC have on the other ASICs part of the chipset
- Possibility to focus the SEU injection on particular module or subsystem and evaluate the effect at system level
- Possibility to inject SEU in hundred of cells per clock cycle (register grouped in non-interacting categories)

Additional checks

- Script to verify that no triplicated instance is optimized out
- Script to verify placement constraints after chip assembly

SSA Single-Event Effect tests with heavy ions

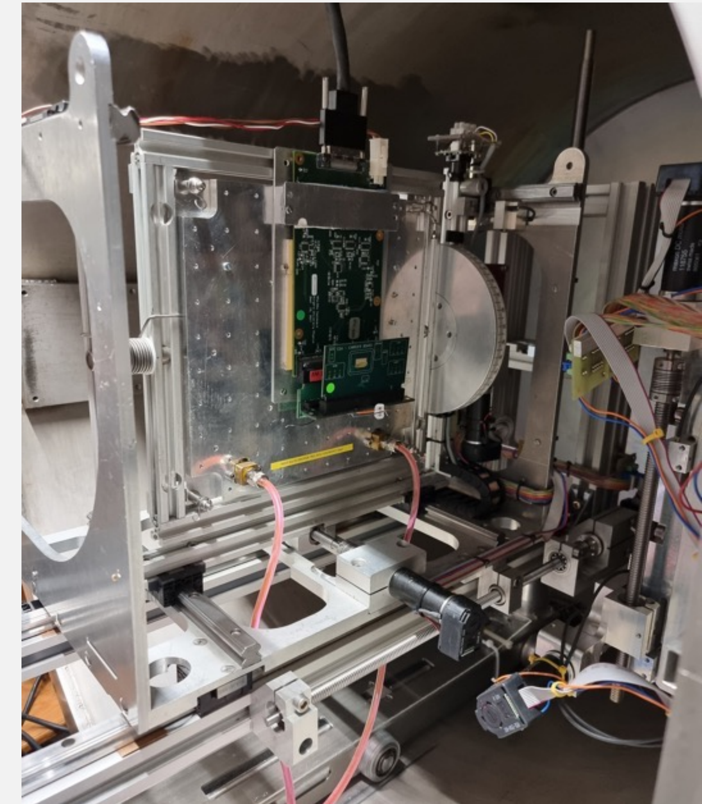
SEE testing carried out in UCL at Louvain-la-Neuve, Belgium

No hard errors observed

- No loss of control observed
- No loss of synchronisation observed
- No chip looks or control errors in general

Configuration system error-free

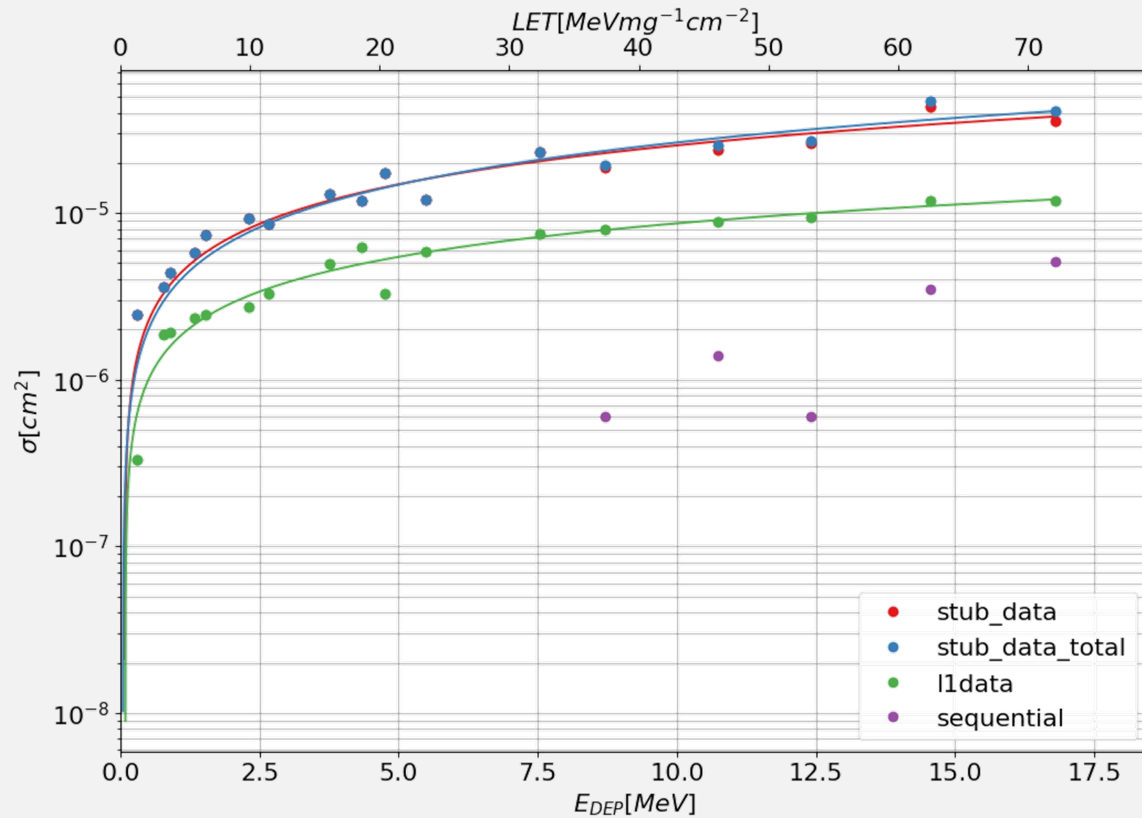
- Verified by readout and comparison of full chip configuration at each test iteration (30 seconds)
- SEU correction counter monitoring



Limit cross section for 10h test ~ **$5 \cdot 10^{-9}$ cm^2**

SSA Single-Event Effect tests with heavy ions

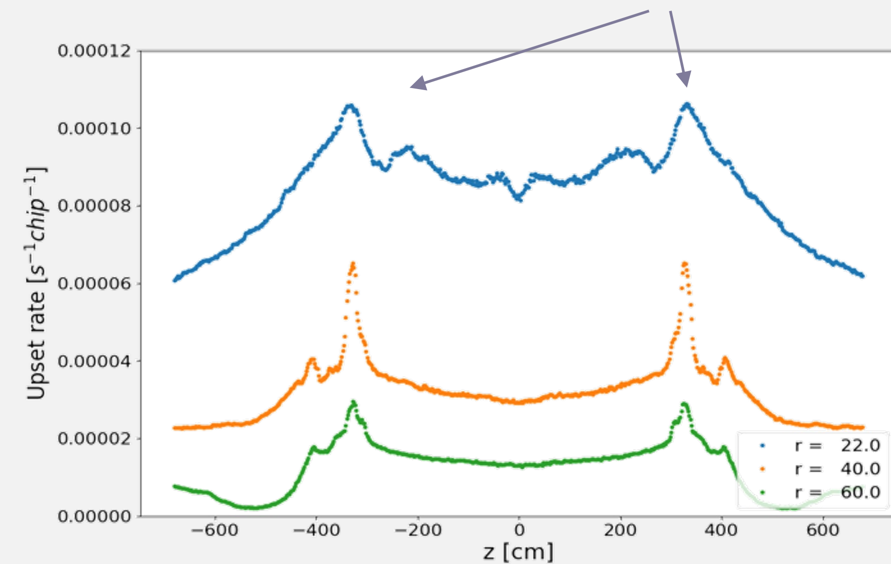
Stub and L1 data SEE cross-section:



Bit error rate estimation

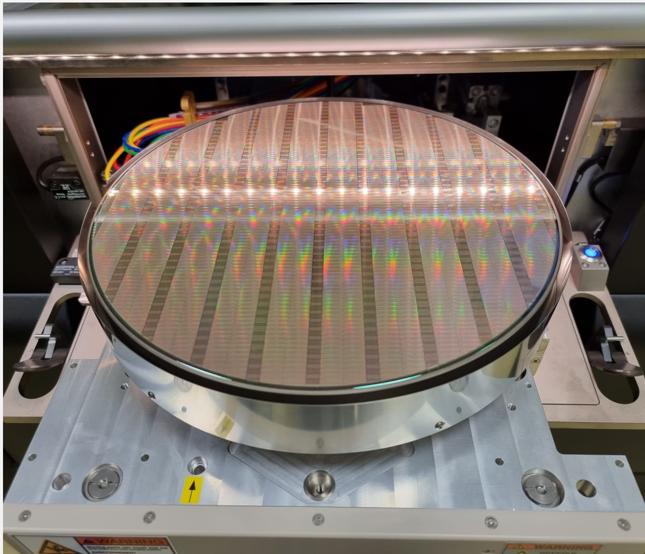
(based on OT fluxes from FLUKA simulation)

	Maximum SSA bit-error rate expected
Stub data	$\mathbf{1.13 \cdot 10^{-3}\ s^{-1}}$
L1 data (12.6 us latency)	$\mathbf{1.04 \cdot 10^{-3}\ s^{-1}}$
L1 data (2.5 us latency)	$9.7 \cdot 10^{-5}\ s^{-1}$



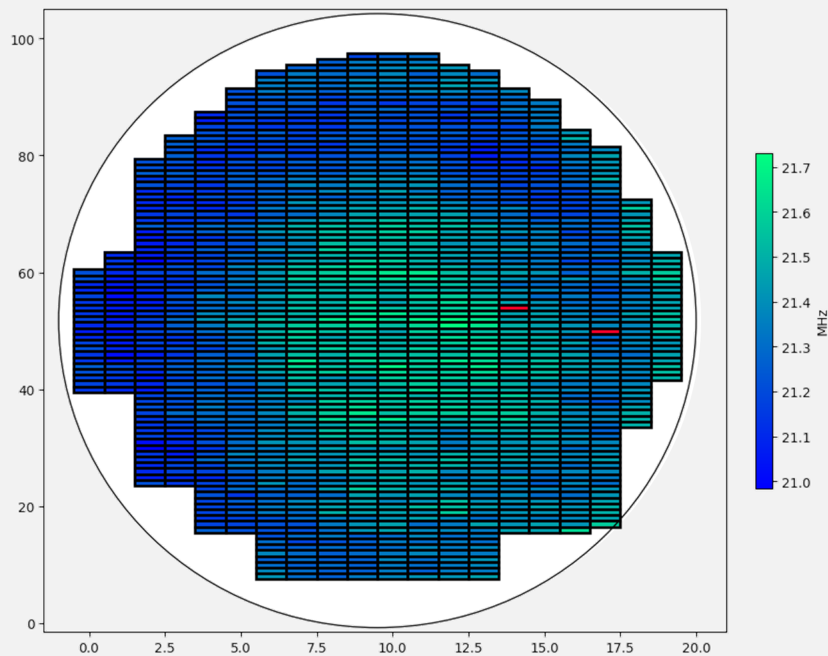
Wafer probing

- The SSA was tapeout in a full mask-set enjeneering run together with the CIC ASIC
- The first 6 wafer have been fully tested
- Test routine includes:
  - Scan-chain test for production defects
  - Functional test of digital circuits
  - Analog bias parameter caracterization
  - Front-end caracterization
  - Noise analysis
  - Serial ID and trimming in e-fuses



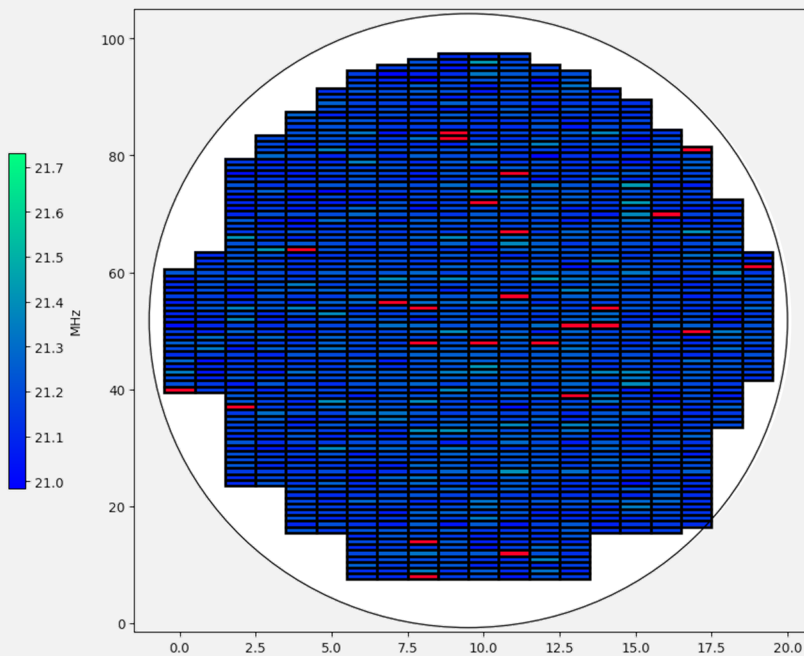
SSA2.1 Wafer Probing - process and analog performance

Ring oscillators Frequency



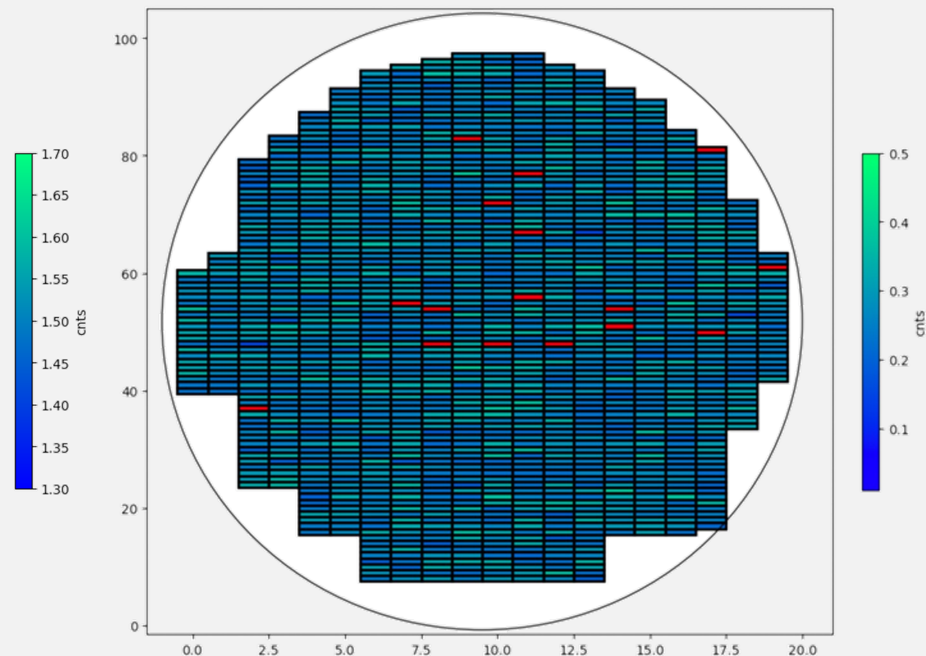
- The SSA includes different types of ring oscillator to monitor variations in: Process – Temperature – Total Ionizing Dose

FE Noise Performance Tests



- Map of the average FE noise
- Cut criteria noise < 1.7 LSB

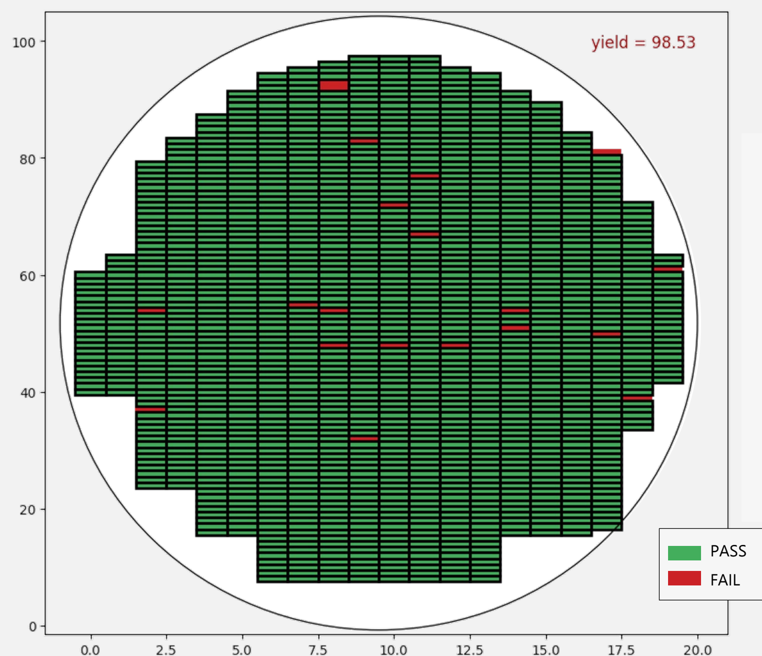
FE Threshold Trimming



- Map of the threshold spread after the trimming procedure
- Cut criteria std(Th) < 0.5 LSB

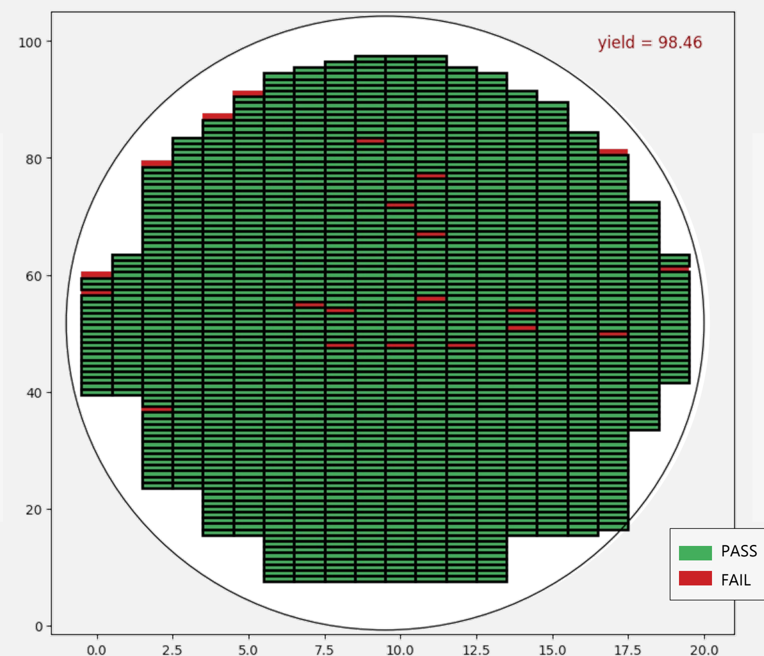
SSA2.1 Wafer Probing - yield

Digital Tests summary map



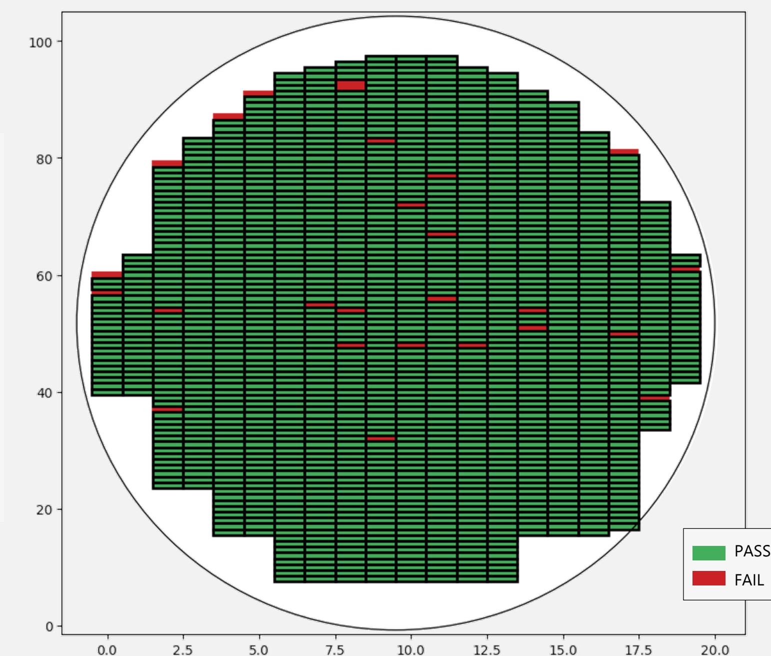
- Stub data [0.9V, 1.0V, 1.1 V]
- L1 data [0.9V, 1.0V, 1.1 V]
- Memory BIST [0.8V, 1.0V, 1.2 V]
- Configuration and all other digital functionalities

Analog Tests summary map



- Analog bias calibration
- FE functionality
- FE Threshold trimming
- Noise analysis

Total yield map



Overall yield (all tests) > 95%

Conclusions

- The final version of the SSA ASIC was summitted for a full mask-set engineering run in 2021
- The first wafer was thinned, bumped and diced allowing for tests on carrier board
- Functional verification and performance characterization results are in line with expectation
- The chip was tested between -40°C and +40°C
- TID test confirms radiation harness up to 200 Mrad
- SEE test with heavy ions shows no loss of control of synchronization
- Wafer level tests show an yield above 94% on the first batch
- The SSA2 together with the MPA2 and CIC2 ASICs enable the assembly of the PS module
- Q3 2023 → Expected delivery of 100 SSA2-CIC2 wafers for a total of 125 000 chips
- Q2 2024 → Expected delivery of additional 75 SSA2-CIC2 wafers for a total of 93 000 chips