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## Performance characterization and radiation tolerance evaluation of the SSA2 ASIC, the strip sensor readout ASIC of the CMS Outer Tracker at the HL-LHC

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This contribution presents the results of the performance characterization and radiation tolerance evaluation of the SSA2 ASIC, the final version of the Short-Strip readout ASIC for the CMS Outer-Tracker PS-module. The ASIC performance is characterised at different temperatures and operating conditions, at the die level as well as at the wafer level. The radiation evaluation comprises Total-Ionising-Dose (TID) tests and Single-Event-Effects (SEEs). Wafer-level testing provided a large dataset to evaluate the production yield. The presented test results are in agreement with the design simulations and are well within the application requirements for operation in the CMS outer-tracker at the HL-LHC.

### Summary (500 words)

The SSA2 ASIC is the final version of the silicon short-strip detector readout ASIC of the CMS Outer Tracker Pixel-Strip (PS) module for the HL-LHC Phase-II upgrades. The SSA2 is a 120-channel ASIC with double-threshold binary readout architecture, utilizing a quick hit cluster finding logic to provide encoded hit information for particle momentum discrimination to the Macro Pixel readout ASIC (MPA) at the bunch crossing rate of 40MHz while allowing the full sensor readout at a nominal average trigger rate of 1 MHz. The on-detector rejection of non-interesting events (or “subs”) allows for a data reduction by a factor of ~20. To match the strict power requirement of 50 mW and the radiation tolerance up to a total ionizing dose of 200 Mrad, low power and radiation hardening techniques have been employed. The SSA ASIC is implemented in a 65 nm CMOS technology.

The functionality and the analog performance of the SSA2 ASIC have been characterised at different operating temperatures (-40C to 60C), operating conditions, and Total Ionizing Dose (TID) levels up to 200 Mrad proving to operate correctly within the tested range. Measurements show an average front-end gain of 54 mV/fC and an average noise of less than 330 e<sup>-</sup> after irradiation, meeting the specification of noise performance. The measured peaking time for an injected charge between 0.5 fC and 8 fC is 19ns +/- 1.6ns, and the time-walk is below 10ns, allowing for detecting consecutive particle events. The embedded trimming circuit allows to obtain a measured threshold spread smaller than 55 e<sup>-</sup> between channels. The measured power consumption is <55 mW and thus within the strict power budget required for operation in the CMS outer tracker PS modules.

During the heavy-ion test campaign with an effective LET on the device of up to 124 MeV cm<sup>-2</sup> mg<sup>-1</sup>, no loss of control, reset, synchronisation or errors on the static configuration have been observed with a limit cross-section of 5E-9 cm<sup>2</sup>. Due to the restricted power budget, the data transmission path on the ASIC is not protected for SEEs and the data error rate is therefore estimated: 7.45E-4 and 5.04E-4 errors per second per chip, respectively for the stub data and for the triggered data in the CMS outer-tracker environment.

The production version of the SSA2 chip has been tested on wafers with an automatic probing procedure, allowing the gathering of a large data set and evaluating the production yield above 95%. Radiation tolerant testability features (scan-chain and built-in self-test) allow to drastically speed up the wafer-level testing process for production defects.

This contribution will present the test bench, the testing methodology and the test results of the functionality,

analog performance characterization and radiation tolerance evaluation of the SSA2 ASIC demonstrating that these results are in agreement with the simulations and fulfil the requirements for operation in the CMS outer-tracker at the HL-LHC.

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