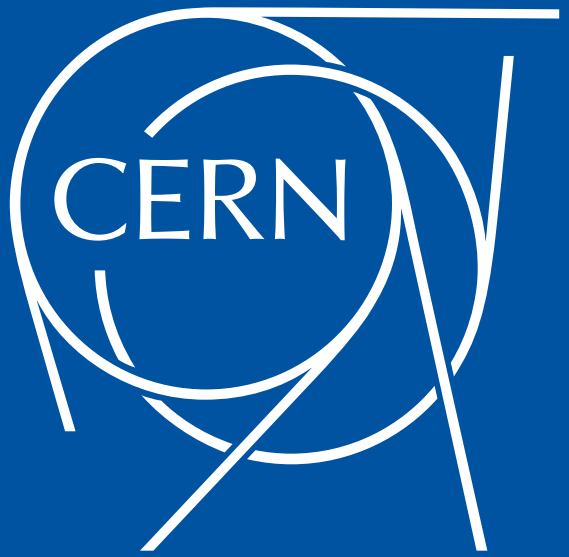
CERN

Analog IP Blocks in 28nm CMOS for the High Energy Physics Community

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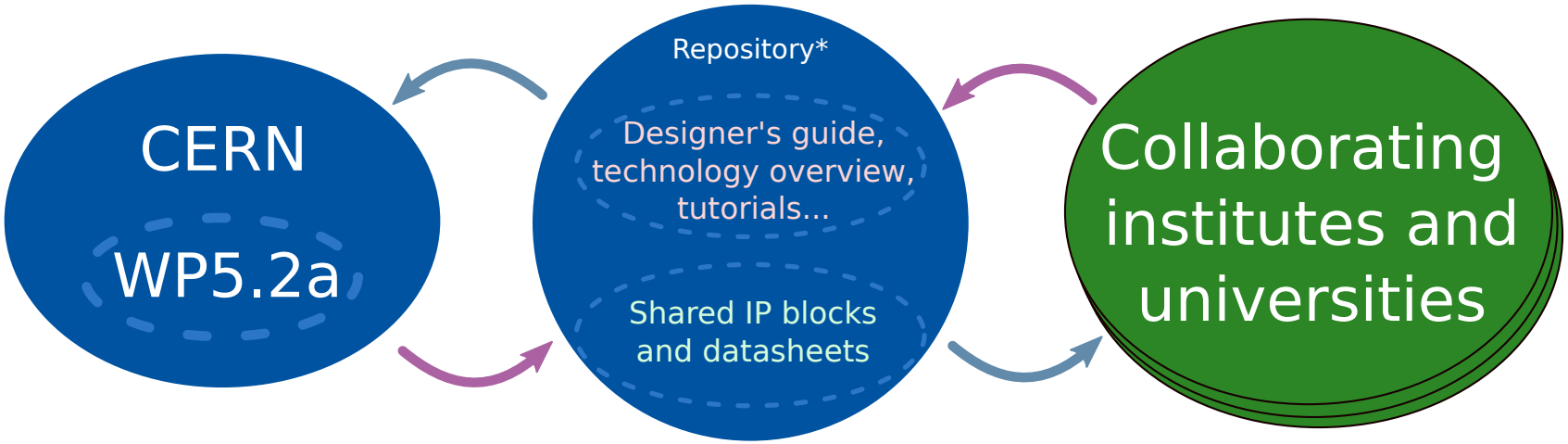
Why IP blocks in 28nm for HEP Community?

This technology is a strong node and will be available in the long term (as 130 nm and 65 nm).



Challenges

Challenges from the technology:

- Low Vdd reduces voltage headroom for analog design.
- DRC rules are very strict:
  - Only vertical poly is allowed (enclosed layout is not possible).
  - Density rules are tough.
  - Dummy filling is required quite early.
- Lot of corners, high mismatch, layout dependent effects...

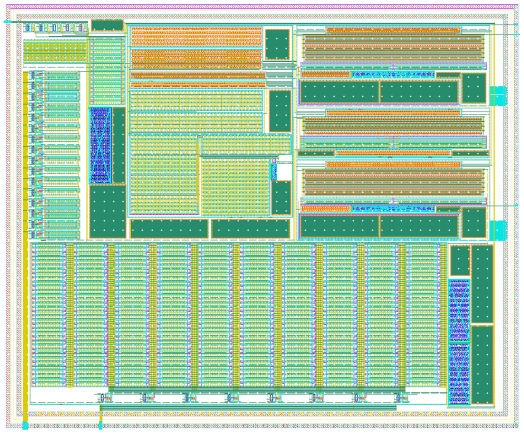
Challenges as a part of a community:

- Communication is important: silicon dimension=90 % drawn dimension.
- Shared IP block should be compatible among them:
  - Several transistor flavours and metal stacks.

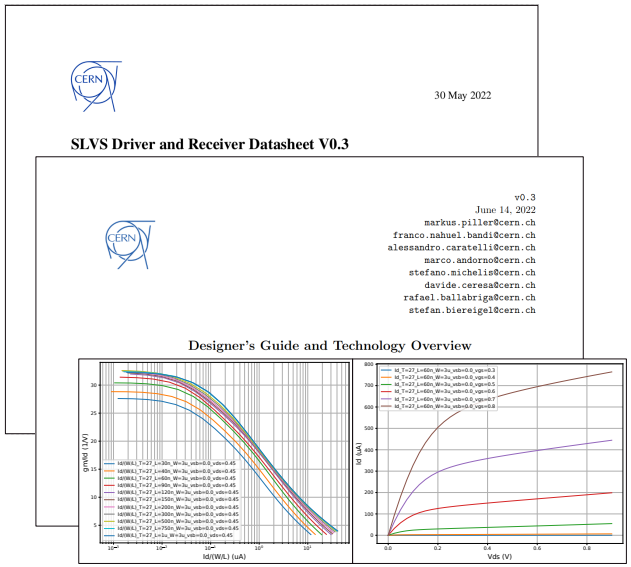
Challenges from the specifications:

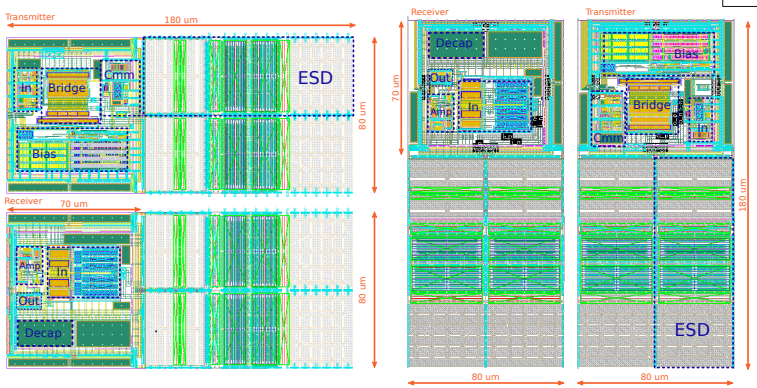
- Up to 1 Grad on 10 years lifetime.

Designers Guide, Technology Overview, Datasheets...

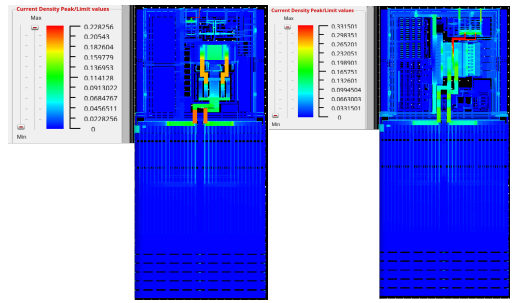


8-bit DAC layout (M. Piller)





Transmitter and receiver layout



Electromigration analysis

[1] The documentation is available (thanks to CERN ASIC Support Team: A. Caratelli and M. Andorno):

- Web page: https://asicsupport.web.cern.ch/
- Forum: https://asicsupport-community.web.cern.ch/

Analog IP Blocks

Conclusions

IP Block Library (Design Finished)

Circuits to share	Notes
Bandgap voltage reference and temperature monitor	Block submitted in January 2022. Development lead by **G. Traversi (Bergamo/Pavia) collaboration with the INFN Falaphel project** with support from CERN engineers.
Digital to Analog Converter (8-bit)	Core block submitted in January 2022. Development lead by M. Piller
Differential line drivers and receivers	Block submitted in January 2022. Development lead by F. Bandi.
Rail to Rail Operational Amplifier	Completed. To be submitted in 2022. Development lead by J. Kaplon.

Design followed guidelines for radiation hardness from the initial technological characterization[1].

[1] Giulio Borghello, "Advantages of 28nm technology in ultra-high-TID environments", *Forum on 28nm CMOS (CERN), Login and access required., 2020.*

Characterization Set-up

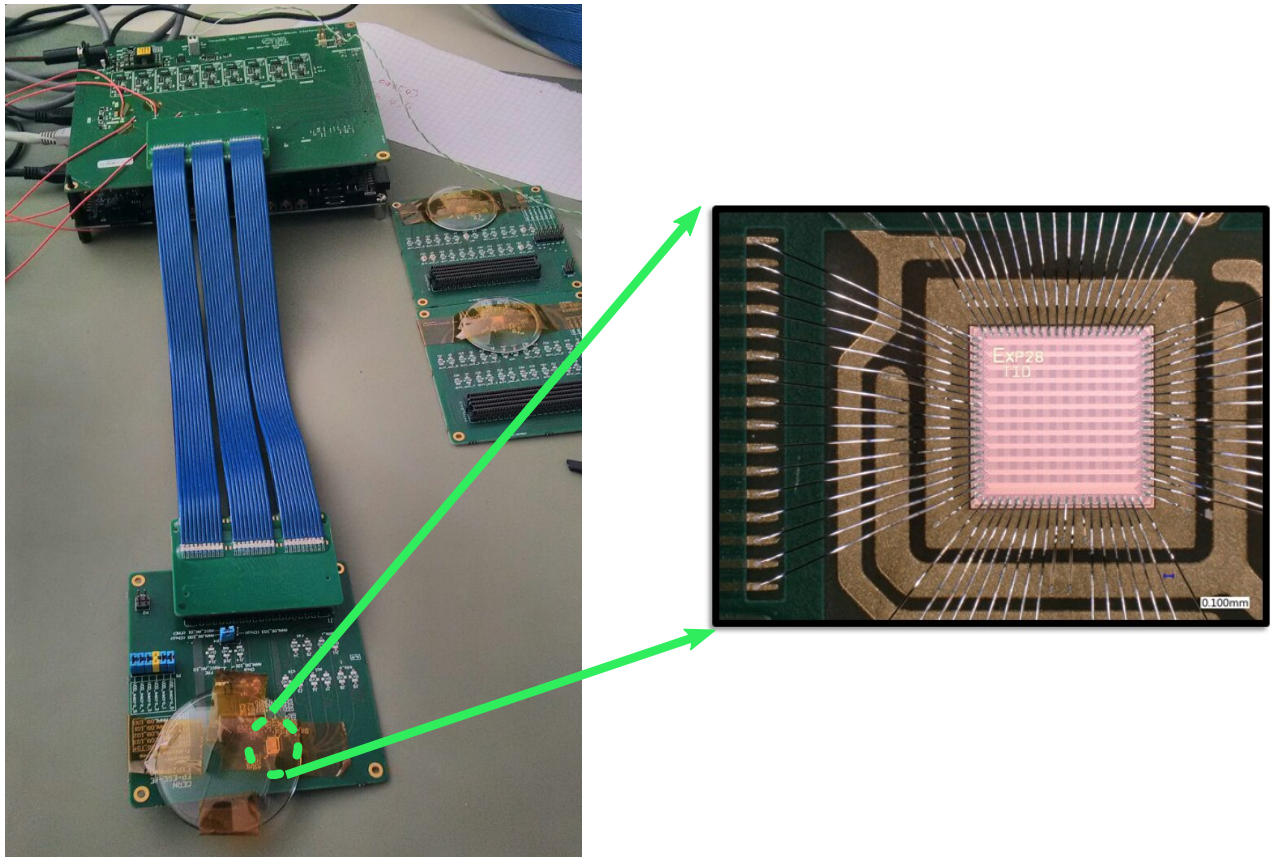
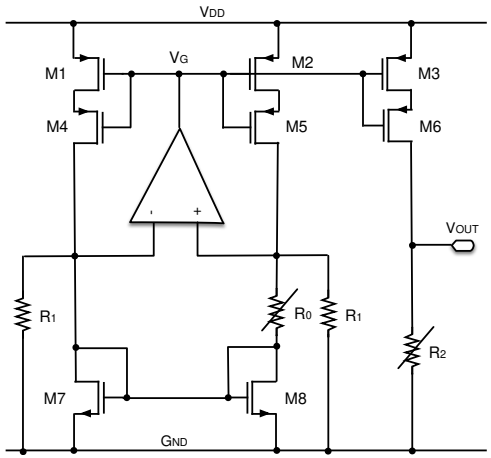


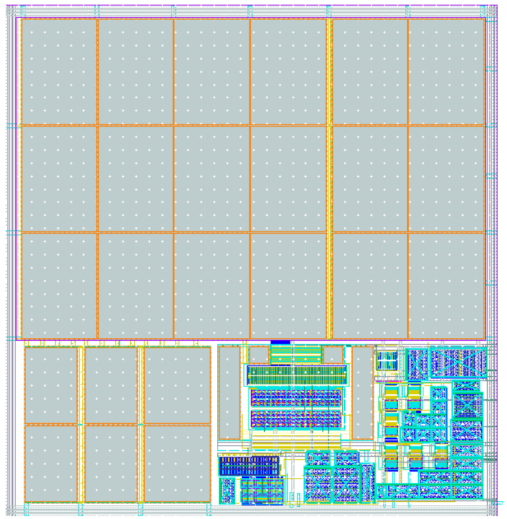
Figure: Left, PCB with wire-bonded chip (bottom) and common test system (top). Right, microphotography of the chip. Acknowledgment: Giulio Borghello, Davide Ceresa, Francisco Piernas Díaz, Risto Pejasinovic.

Bandgap Voltage Reference (by G. Traversi)

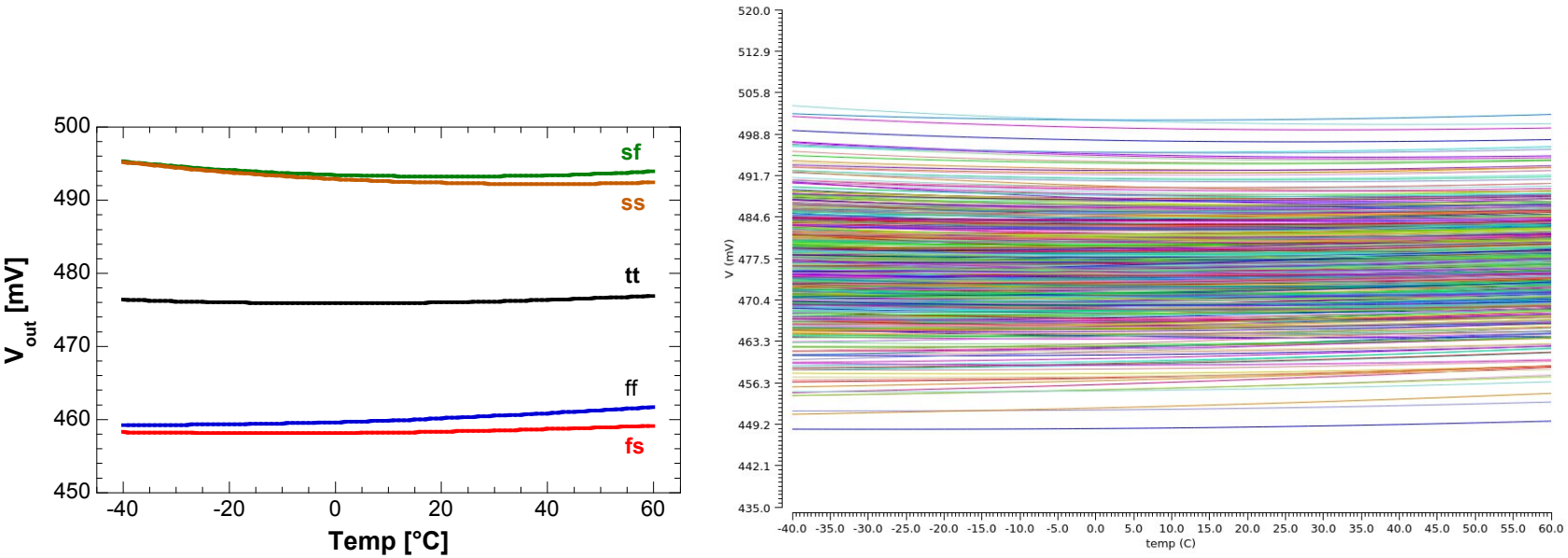
Designed by **Bergamo-Pavia in collaboration with the INFN Falaphel project (Main designer: G. Traversi)** and technical support from CERN.



Parameter	Min	Typ	Max	Unit
Voltage supply	0.81	0.9	0.99	V
Output voltage		480		mV
Current supply		100		µA
Temperature	-40	25	60	°C
ΔVref max vs Temp		3		mV
ΔVref max vs Vdd±10 %		2		mV
Target PSR (low frequencies)		40		dB
Active element	lvt in weak inversion			



Bandgap: Simulation Results



(a) (b)

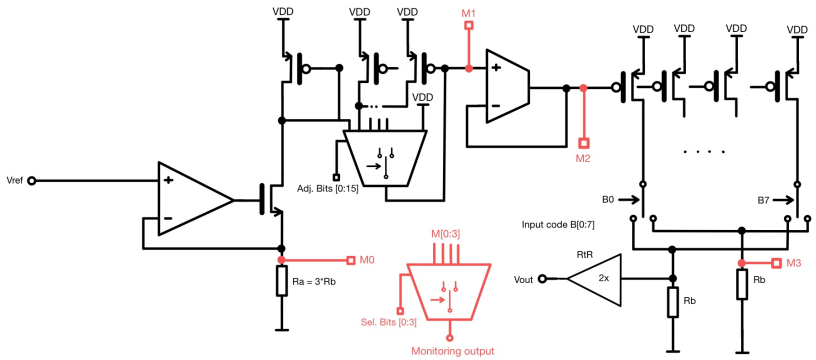
Figure: (a) Output voltage as a function of the temperature (corners). (b) Output voltage as a function of the temperature (mismatch)[2]. Experimental characterization will start in the following weeks.

[2] G. Traversi, et al., "Design of a Radiation-Tolerant Bandgap Voltage Reference for HEP applications", *2022 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, Milano.

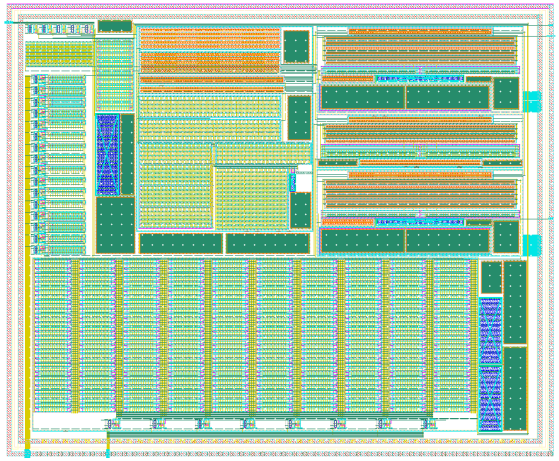
8 Bit DAC (by M. Piller)

The 8 bit digital-to-analog converter is intent to be a IP block for biasing purposes.

- 8 bit digital-to-analog conversion.
- Output voltage before RtR 0 to $V_{DD}/2$.
- INL < 0.5.
- I_{LSB} digital current adjustment.
- $I_{LSB} = 50nA$.



Parameter	Min	Typ	Max	Unit
Voltage supply	0.81	0.9	0.99	V
INL			0.38	
Temperature	-40	25	80	°C
Area		220×267		μm^2
Metal stack		1-2-3 (4,5 power)		metals



DAC: Experimental Results

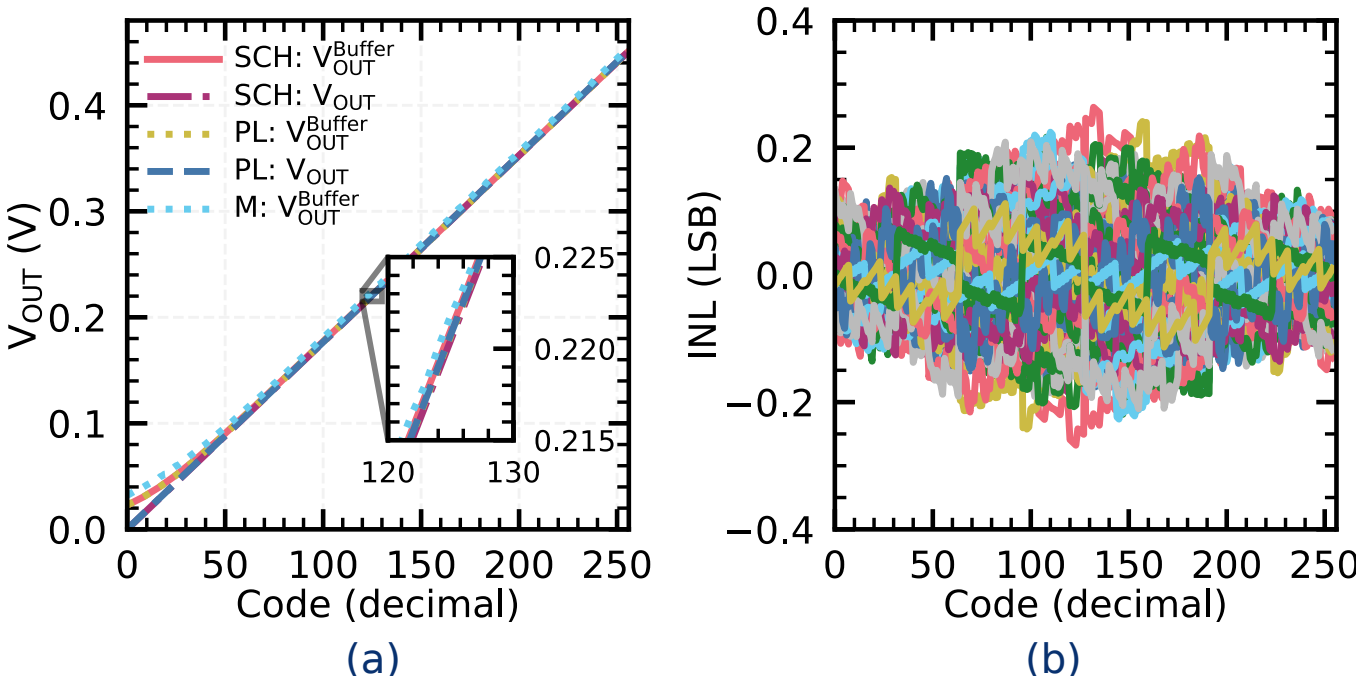


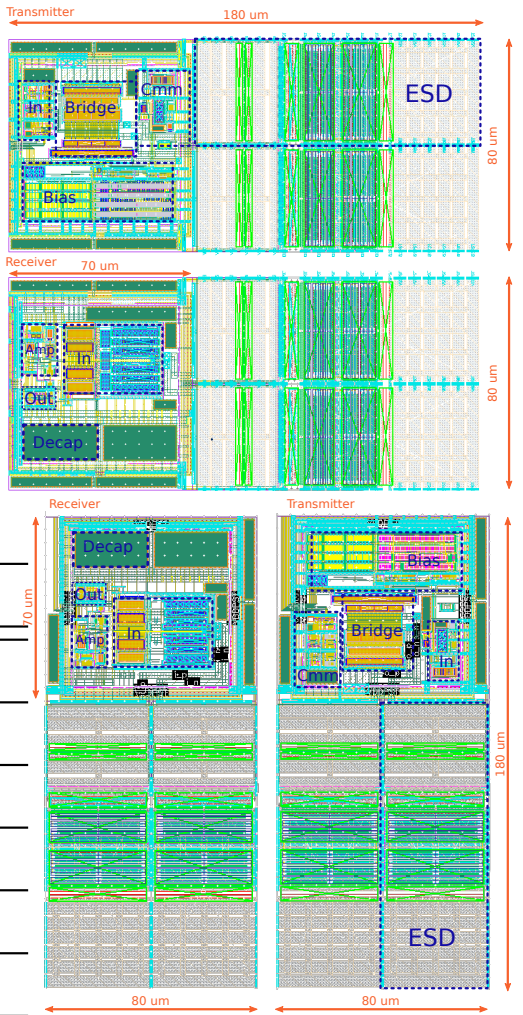
Figure: (a) DAC output voltage results from schematic and post layout (PL) simulations and measurements (M) (b) Calculated INL from Monte Carlo simulations[3]. Irradiation will start in the following weeks.

[3] M. Piller, et al., "Generic Analog 8 Bit DAC IP Block in 28nm CMOS for the High Energy Physics Community", *2022 Austrochip Workshop on Microelectronics (Austrochip)*, 2022.

SLVS Transmitter and Receiver (by F. Bandi)

The design targets mainly on-board chip-to-chip communication in rad-hard applications (1 Grad). Therefore, only thin-gate transistor should be used to ensure higher radiation tolerance [3].

- Disable signal.
- Inverter function.
- Compatible with low voltage design ($V_{ddcore} = 0.8\,V$).
- Level shifting: from V_{ddcore} to V_{ddIO}.
- Tx: $I_{out} = 4\,mA$.
- Rx: termination on/off switch and fail-safe resistors.



Parameter	Min	Typ	Max	Unit
IO voltage supply	1.08	1.2	1.32	V
Core voltage supply	0.72	0.9	0.99	V
Data rate	0		1.28	Gbps
Temperature	-40		80	°C
Area with ESD		180×80		μm^2
Metal stack		1-2-3(4 power)		metals

SLVS: Experimental Results

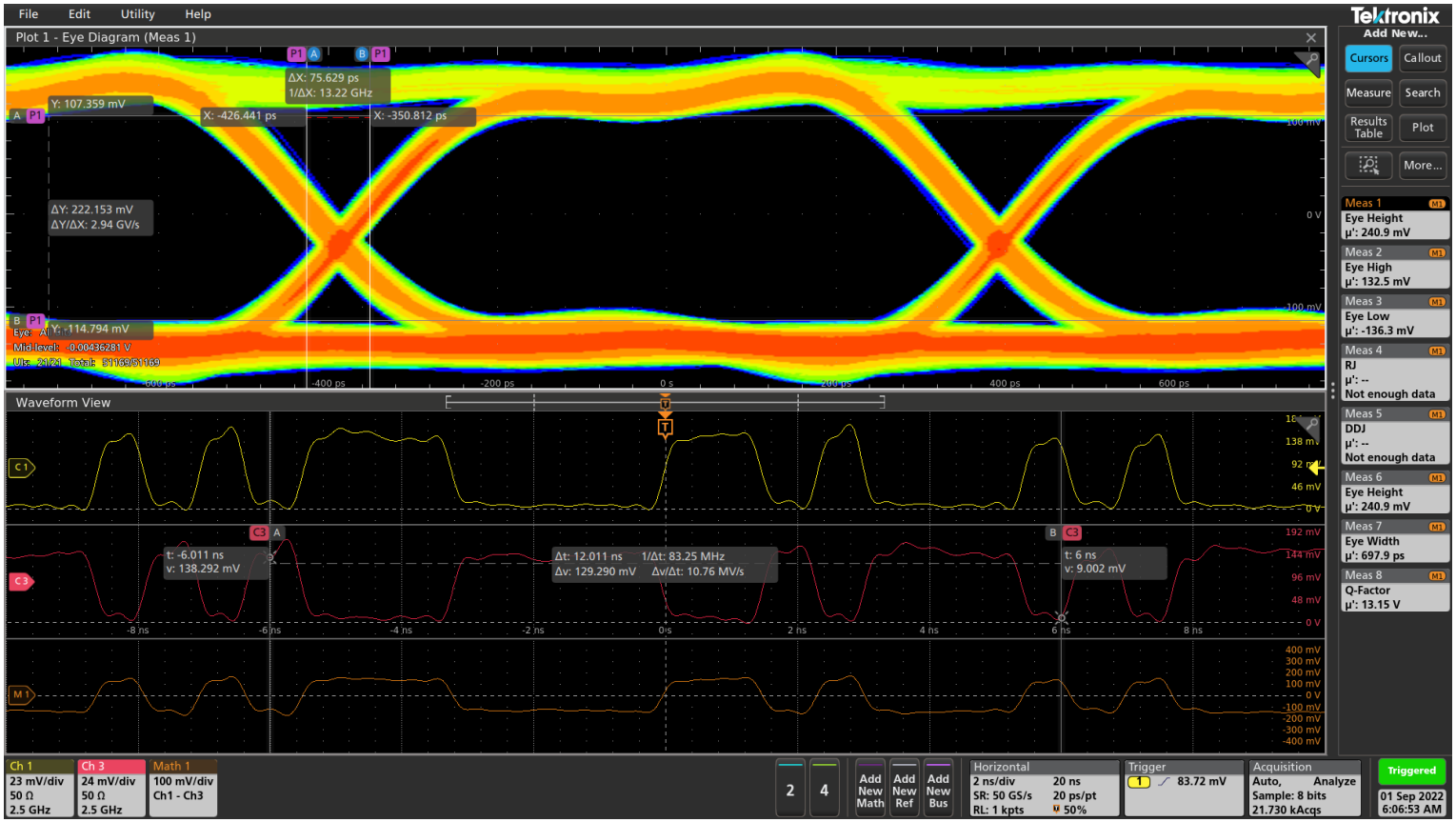


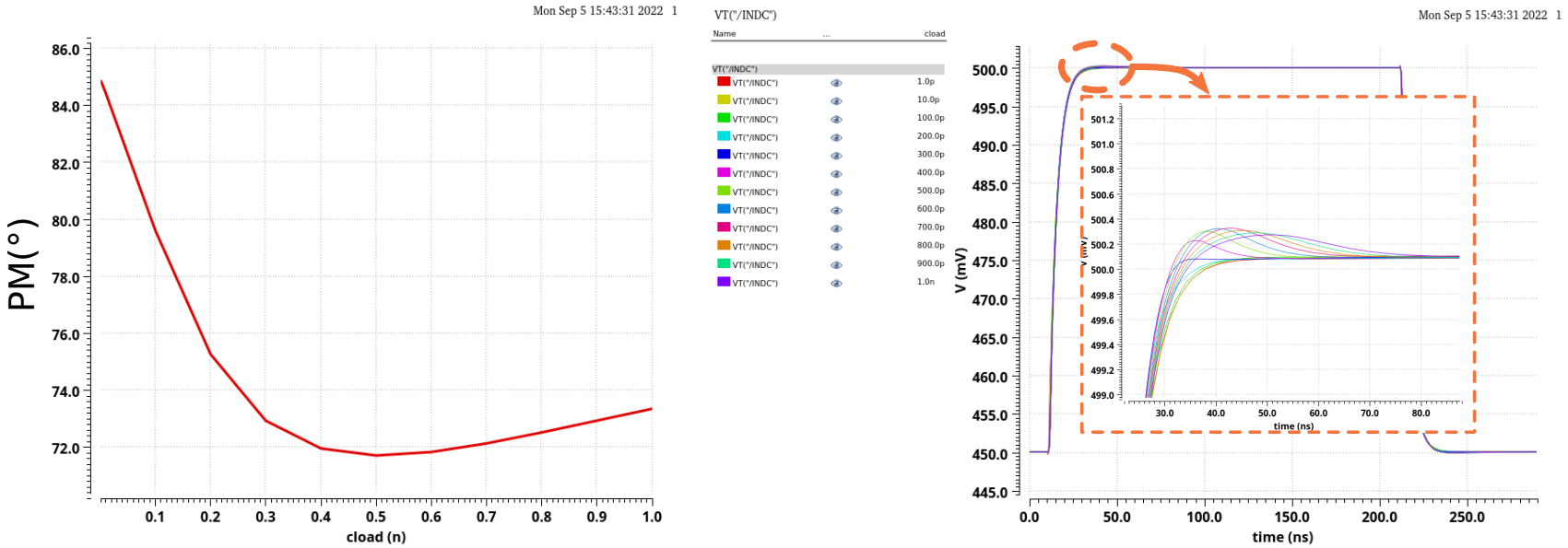
Figure: Eye diagram at 1.28 GHz with 100 Ω termination impedance (oscilloscope input impedance). Eye height, width and jitter are 240 mV, ∼ 700 ps and ∼ 80 ps, respectively. No significant degradation after 1Grad. Acknowledgment: G. Borghello, D. Ceresa, F. Piernas Díaz, R. Pejasinovic.

Rail to Rail OPAMP (by J. Kaplon)

Parameter	Min	Typ	Max	Unit
Open loop Gain	70	75		dB
GBP (uncompensated)		1.6		GHz
Current supply			400	µA
PM (unity gain for 0-1nF load and 10 Ω series resistor required)	66	74		°
Settling time (1 %)[4]			35	ns
Output noise (unity gain)			150	µV
Offset rms (unity gain)			1.5	mV
Area (amplifier and bias)		$44 \times 70 + 44 \times 90$		μm^2
Area (amplifier, bias, decoupling and compensation)[4]		140×160		μm^2

[4] Unity gain configuration.

OPAMP: Simulation Results



(a) (b)

Figure: (a) Phase margin as a function of load capacitance for unity gain configuration. (b) Transient response for unity grain configuration for 50mV step at the input.

IP Block Library (Work In Progress)

Circuits to share	Notes
Analog to Digital Converter for monitoring (12b incremental 16b free running; Volt/curr mode)	In progress. Development lead by T. Hofmann. Collaboration with University of Ulm.
Rail to Rail Operational Amplifier (slow/low power (e.g. monitoring in unity gain))	In progress. To be submitted in 2022. Development lead by M. Piller.
Digital to Analog Converter (10-bit)	Development lead by V. Sriskaran.
Digital PLL	Discussion on specifications ongoing, collaboration with WP6.
DCDC converter	In progress. Development lead by S. Michelis and G. Ripamonti
LDO	In progress. Development lead by TU Graz, supervised by S. Michelis
Shunt LDO (SLDO) for serial powering solutions (mainly inner tracker pixels)	In progress. Development lead by M. Karagounis (FH Dortmund)

Analog IP Blocks

Conclusions

Conclusions

- Some IP blocks were submitted in January 2022 and more circuits are under design.
- The IP blocks are accompanied by datasheets. A designer's guide and other support documents have been prepared to assist designers.
- We have created synergies with other groups in the community.
- After a total ionizing dose of 1Grad, the SLVS transmitter and receiver meet specifications.
- The other blocks will be characterize and irradiated in the following weeks.

Bibliography

[1] G. Traversi, et al., *Design of a Radiation-Tolerant Bandgap Voltage Reference for HEP applications*, 2022 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Milano.

[2] M. Piller, et al. , *"Generic Analog 8 Bit DAC IP Block in 28nm CMOS for the High Energy Physics Community"*, 2022 Austrochip Workshop on Microelectronics (Austrochip), 2022.

[3] Giulio Borghello, *Advantages of 28nm technology in ultra-high-TID environments*, Forum on 28nm CMOS (CERN), Login and access required., 2020. https://indico.cern.ch/event/970389/contributions /4097899/attachments /2141534/3608590/Advantages%20of%2028nm %20CMOS%20Technology%20in%20Ultra-High-TID%20Environments %20-%20Giulio%20Borghello.pdf

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