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Analog IP Blocks in 28nm CMOS for the High Energy Physics Community

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A bandgap voltage reference, an 8-bit binary-weighted Digital to Analog Converter (DAC), a rail-to-rail operation amplifier and a scalable low voltage signaling (SLVS) transmitter and receiverhave been developed as macro blocks in 28 nm CMOS technology for the future upgrades for the high luminosity LHC. This work summarizes the design approach at the schematic and layout level. Practical aspects of the novel technology for the design of ASICs in high energy physics will be discussed in the contribution along with characterization results.

Summary (500 words)

The requirements for the future upgrades for the high luminosity LHC impose a radiation hardness up to 1Grad and hit rates in the order of 3GHz/cm2 in the inner layers of the detectors [1]. With such specifications, ultra-deep submicron technologies become an appealing option to integrate circuits because of their inherent radiation tolerance, high transistor density, low power consumption, and faster operation frequency. One of the activities in Work Package 5 of the CERN EP R&D program consists of designing and characterizing macro blocks in 28nm CMOS technology for the HEP community.

The bandgap voltage reference provides an output voltage of 450mV with a PSRR of 40dB while consuming 100µA. The maximum voltage reference variation with a supply variation of ±10% is 2mV, while for temperature variations from −40◦C to 60◦C, it is 3mV. A low voltage threshold NMOS transistor in weak inversion is used as active element.

The 8-bit binary weighted Digital to Analog Converter (DAC) has a least significant bit size of 50nA, which is digitally adjustable to compensate for process, voltage, and temperature variations. The INL is below 0.5LSB. The output voltage before the output buffer swings from 0 to Vdd/2. The output buffer is implemented with a rail-to-rail operational amplifier (OPAMP) in a ×2 configuration. The total area of the DAC is 220×267µm2.

The rail-to-rail OPAMP has an open-loop gain of 75dB with a gain product bandwidth of 1.6GHz while consuming 400µA. The phase margin is 74°, and the setting time is achieved after 35ns. In unity gain configuration, the output noise is 150 µV and the offset rms is 1.5mV. The total area of the OPAMP—including bias, decoupling, and compensation—is 140×160µm2 . A second rail-to-rail OPAM with smaller bandwidth is under development for monitoring purposes.

Finally, the scalable low voltage signaling (SLVS) transmitter and receiver target on-board chip-to-chip communication, a data rate of 1.28Gbps and a maximum transmitter output current of 4mA. The transmitter architecture is based on a PMOS-over-NMOS H-bridge. Its common mode control is provided by a scale replica circuit. The receiver architecture is based on a self-bias differential amplifier provides wide input swing and rail-to-rail output [2]. Passive fail-safe resistors are implemented in the input stage to define a valid state when the input signal is unavailable. The core of each circuit occupies 70×70µm2 , and the total area becomes 180×80µm2 when the electrostatic discharge protection diodes (implemented by an external company) are included.

All circuits were designed with thin-oxide transistors to increase radiation tolerance. The core circuitry is nominally powered with 0.9V, with the only exception of the transmitter's output that is powered with 1.2 V to provide compatibility with previous designs.

References
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[2] S. Bonacini, K. Kloukinas, and P. Moreira, "E-link: A Radiation-Hard Low-Power Electrical Link for Chip-to-Chip Communication,"2009. [Online]. Available: https://cds.cern.ch/record/1235849

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