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HKROC: an integrated front-end ASIC to readout photomultiplier tubes for the Hyper-Kamiokande experiment

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HKROC is an ASIC designed to readout the photomultiplier tubes of the Hyper-Kamiokande experiment. With a large number of channels and stringent readout requirements in terms of noise, speed and dynamic range, the ASIC is very challenging and innovative. Each HKROC channel embeds low-noise preamplifier-shapers, a 10-bit SAR-ADC for the charge measurement (up to 2500 pC) and a TDC for the Time-of-Arrival (ToA) measurement with 25 ps binning. HKROC is auto-triggered and includes all necessary ancillary services as bandgap circuit, PLL and threshold DACs. We will present the experimental results of the first HKROC prototype received in January 2022.

Summary (500 words)

HKROC (Hyper-Kamiokande ReadOut Chip) is the ASIC designed to read out the large number of PhotoMultiplier Tubes (PMT) of the future Hyper-Kamiokande experiment. This chip is based on the developments performed for the HGROC chip (for the CMS experiment) modified to fulfill Hyper-Kamiokande needs.
The first prototype of HKROC was submitted (TSMC 130 nm) in August 2021 and lab tests have been conducted since January 2022.
HKROC is a complex system-on-chip with analog and digital processing. It embeds 36 independent channels working in a trigger-less fashion.
To cope with the Hyper-Kamiokande large dynamic range (up to 2500 pC), each PMT is connected to three channels of the ASIC. The dynamic range is split into three parts corresponding to different channel gain configurations (High, Medium or Low gain). Thus, from a system point of view, one HKROC can be connected to 12 PMTs.
HKROC trigger-less mechanism is based on an internal trigger generated according to the input signal level. Each channel of the chip is made of a low-noise input preamplifier followed by two paths: a fast path with a discriminator connected to 10-bit Time-to-Digital Converter (TDC from CEA IRFU group) for time measurement with 25 ps accuracy; a slow path with shapers connected to a 10-bit 40 MHz successive approximation Analog-to-Digital Converter (SAR ADC from AGH Krakow) for charge measurement up to 2500pC.
The TDC is only activated when the input signal is higher than a defined threshold. When triggered, it opens an acquisition window where all input signals are digitized, stored and automatically read out. The TOA is directly given by the TDC. For the charge, the shaper output is continuously sampled by the ADC at 40 MHz. Only during the acquisition window, the digitized samples are stored inside a memory (with a maximum of 32 samples).
The ASIC intends to be a versatile readout chip and it has many configuration registers to tune its behavior. The parameters can be loaded and verified through a standard I2C protocol: all the internal parameters are triplicated for redundancy.
Many clocks are required internally for sub-modules (I2C, ADC, TDC): they are all derived from one incoming 320 MHz clock thanks to an internal PLL. An incoming bit-stream is attached to this clock and can be used to send fast commands to control some specific parts of the circuit: link synchronization, reset, calibration, etc.
The digital processing of the circuit is handled at 40 MHz (also derived from the incoming 320 MHz): to limit

the coupling of the digital activity on the analog part, a phase-shifted 40 MHz is created internally and sent to all the digitizers (ADC and TDC). By default, the chip works in a trigger-less and autonomous mode. All the relevant data (charge and time) are stored into local memories (depth 32) and then readout through four high speed differential links working at 1.28 Gbps. The ASIC characterization shows a good overall behavior. The ASIC architecture, the performances and the PMT measurements will be presented.

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