NEVIS LABORATORIES
COLUMBIA UNIVERSITY

The COLUTA ADC ASIC and the ATLAS HL-LHC Liquid Argon Front-End Readout

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O.B.O the ATLAS Liquid Argon Calorimeter Group

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Outline

- ATLAS LAr Calorimeter & the High-Luminosity LHC Upgrade
- COLUTAv4 ADC
- Front-End Board “2” (FEB2)
- Conclusions

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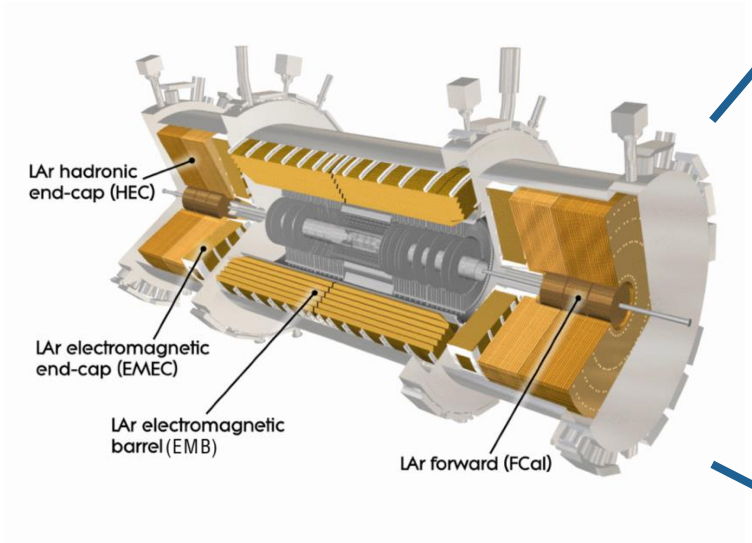
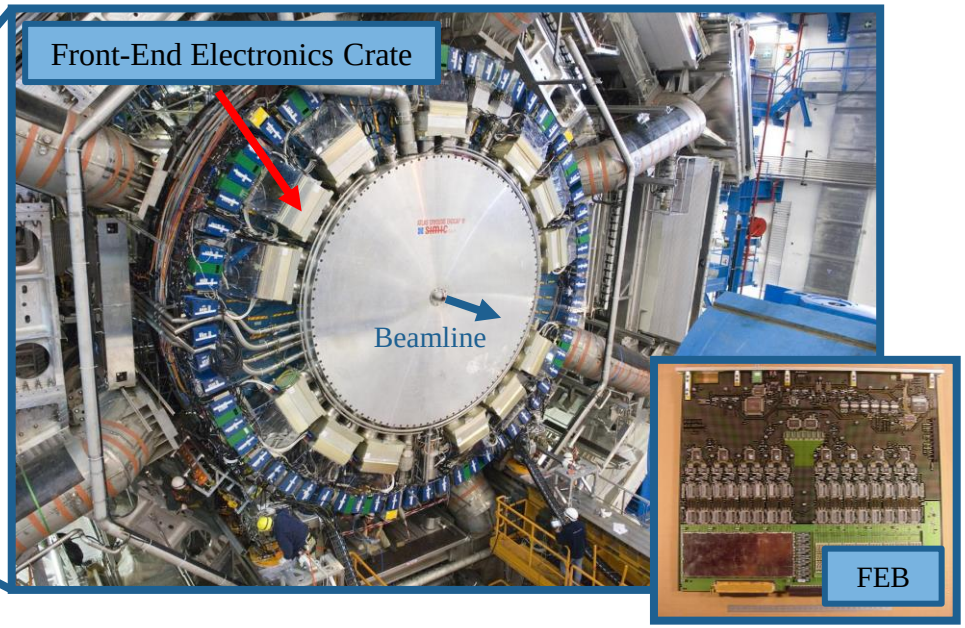
ATLAS LAr Calorimeter

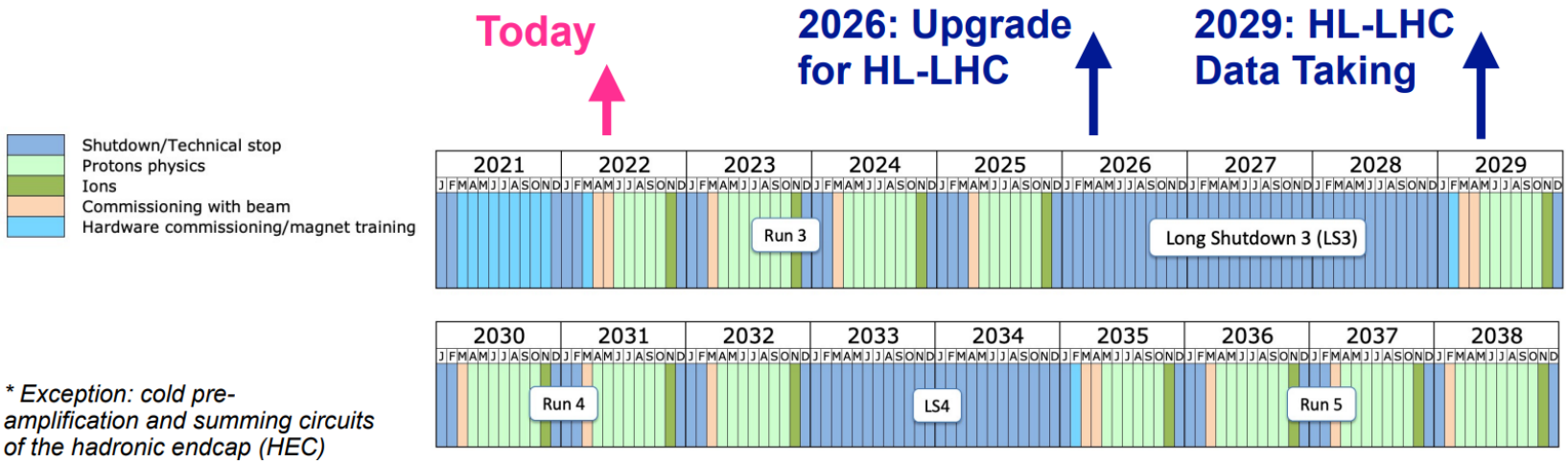
- ATLAS LAr calorimeter captures energy and timing info of EM and hadronically interacting particles
- Calorimeter divided into EM barrel, the EM and hadronic end-caps, and forward calorimeter
- Readout electronics system samples cells at LHC frequency of 40 MHz and sends digitized pulses of interactions off the detector for signal analysis and triggering
  - Front-end boards (FEBs) are located on cryostat for optimal analog performance: high radiation, high magnetic field, limited access
  - Off-detector electronics apply digital filtering to extract energy and time for each cell, pass info to trigger & DAQ





The High Luminosity LHC

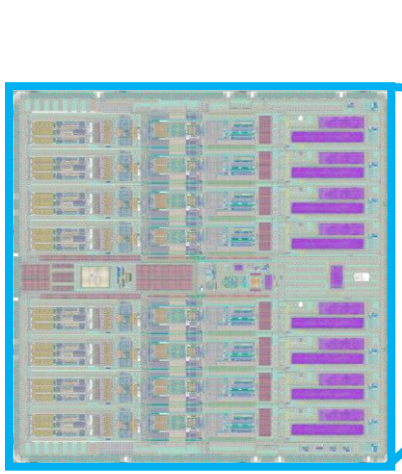
- ❖ High Luminosity LHC (HL-LHC) scheduled to begin operation in ~2029
  - Will allow for up to 7x design luminosity (~200 simultaneous collisions) and provide access to very rare new physics processes and more precise measurements of the Higgs coupling
- ❖ Original on-detector electronics good up to 1,000 fb^{-1} (out of the 4,000 fb^{-1} expected for HL-LHC)
  - Expect a 200x increase in readout data rate + stringent radiation requirements
  - To accommodate the HL-LHC data volume and for ageing components, need to replace **all readout electronics (1524 FEBs, 120 calibration boards, off-detector components)***



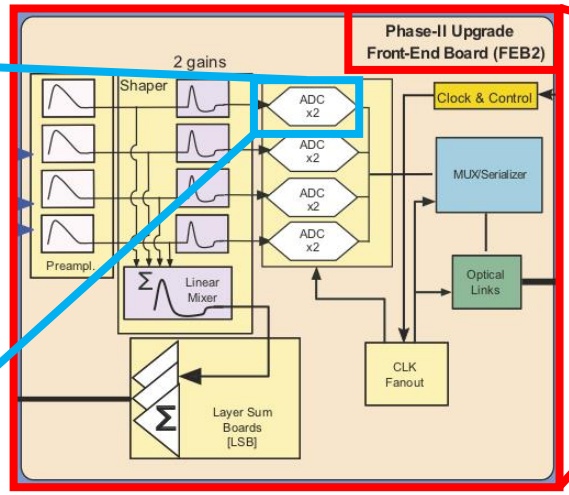
** Exception: cold pre-amplification and summing circuits of the hadronic endcap (HEC)*

HL-LHC LAr Calorimeter Front-End Readout

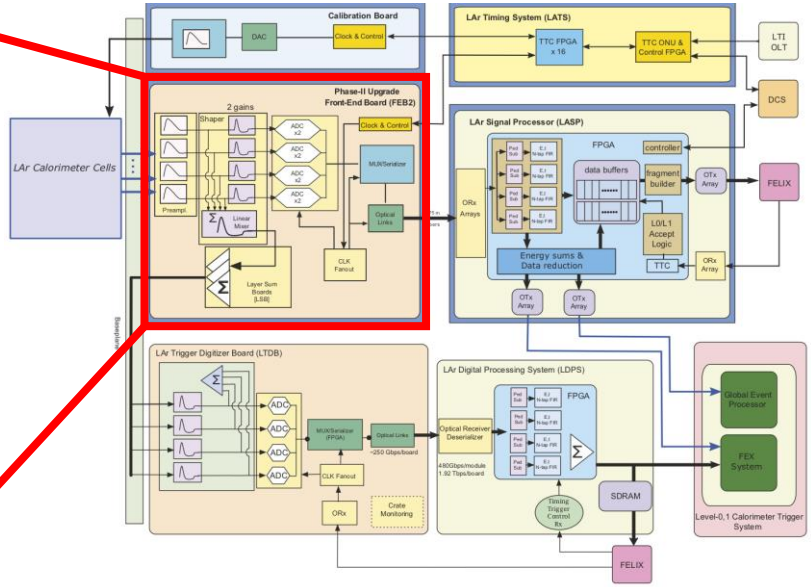
- Front-end readout at the HL-LHC provided by Front-End Board "2" (FEB2) boards
- Design requires implementation of custom-built ASICs due to radiation tolerance requirements
  - 16-bit dynamic range pre-amp/shaper (PA/S) with two gain scales (hi/lo~25), ADC, and lpGBT 10 Gbit/s serializers
- **This talk will focus on the performance of the COLUTA LAr ADC + give a brief overview of the development and testing of the FEB2s**



COLUTA ADC



Front-End Board 2 (FEB2)



LAr Calorimeter Readout Architecture

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- ATLAS LAr Calorimeter & the High-Luminosity LHC Upgrade
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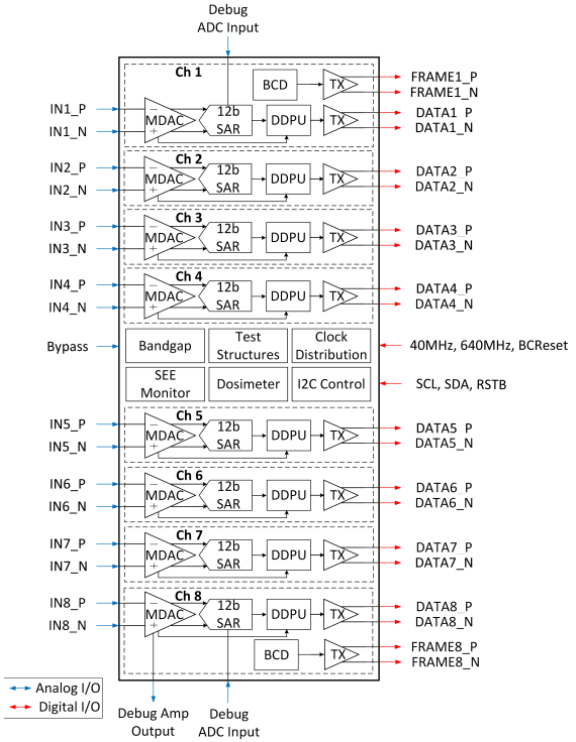
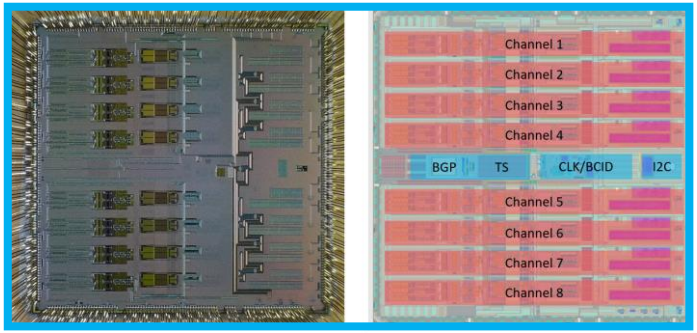
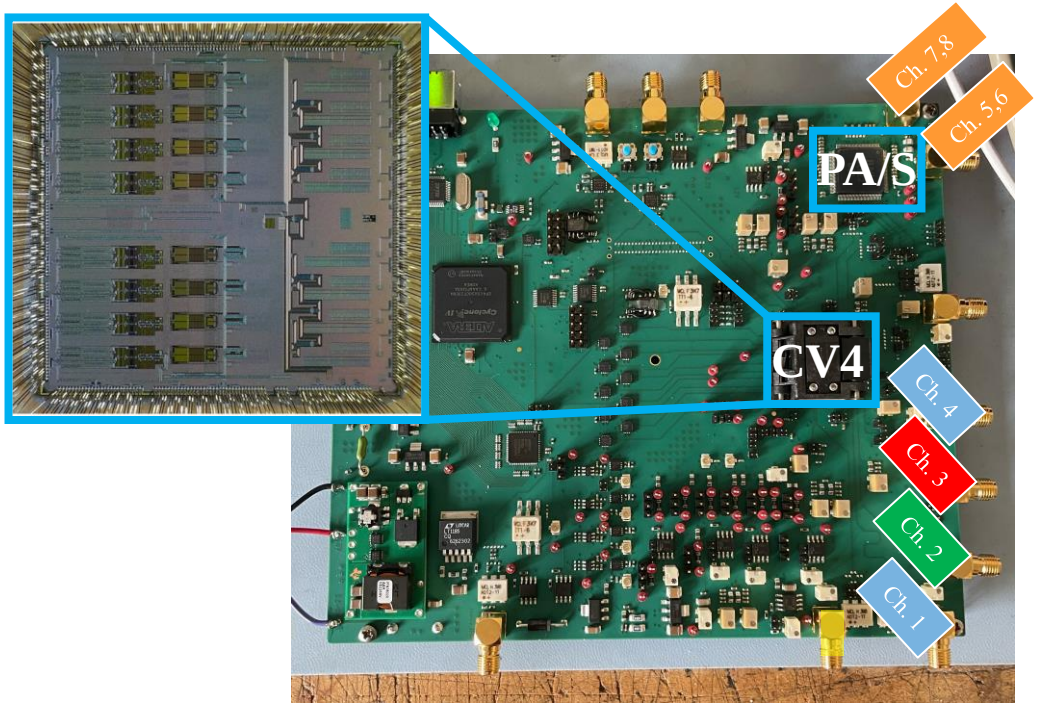
COLUTAv4 (CV4) ADC Overview

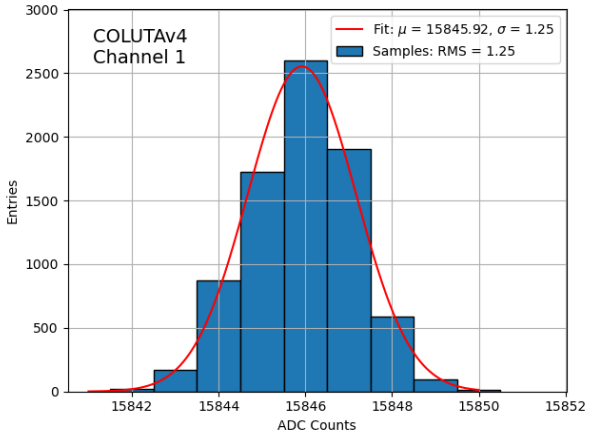
- Final prototype (4th iteration) of full custom COLUTA ADC ASIC
- 8-channel, 15-bit, A/D converter
  - 3.5-bit Multiplying DAC (MDAC) followed by 12-bit Successive Approximation Register (SAR)
  - Digital Data Processing Unit (DDPU) applies calibration bit weights and serially transmits data at 640MBPS
- TSMC 65nm LP CMOS
  - 5.585 x 5.454 mm^2 chip die
  - 4.3 million transistors
  - 1.2 V operation with 2 V_{pk-pk} differential input
- Digitizes both lo/hi gains of LAr calorimeter channels
  - Digitization at 40 MSPS
  - ≥14-bit dynamic range and >11-bit ENOB precision
  - Seamless interface to PA/S, lpGBTs
  - On-chip calibration circuit for MDAC and SAR
    - Derived calibration weights stored in DDPU
  - Radiation tolerance for HL-LHC

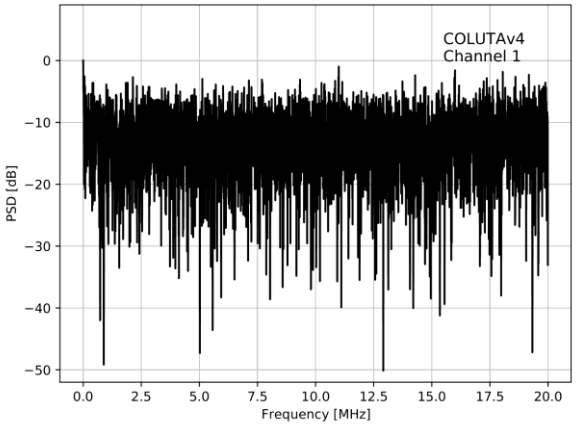




Test Setup & Noise Measurements





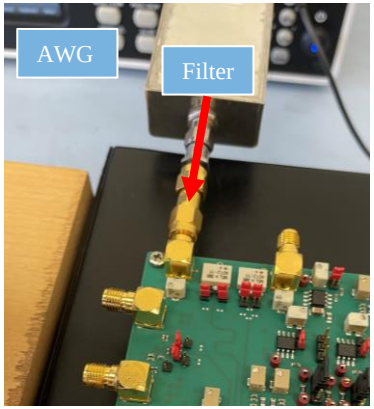


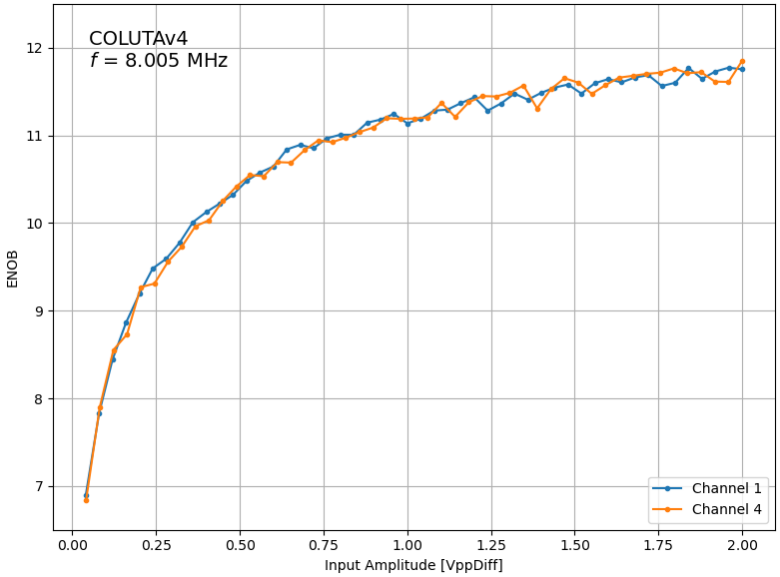
- CV4 testboards with either socketed or soldered chip
  - Chs. 1, 4: transformer input
  - Ch. 2: commercial amplifier input
  - Ch. 3: connected to 16-bit onboard DAC
  - Chs. 5-8: connected to PA/S prototype
    - 5,8 → lo gain; 6,7 → hi gain
- Socketed board used for QA/QC, soldered for performance

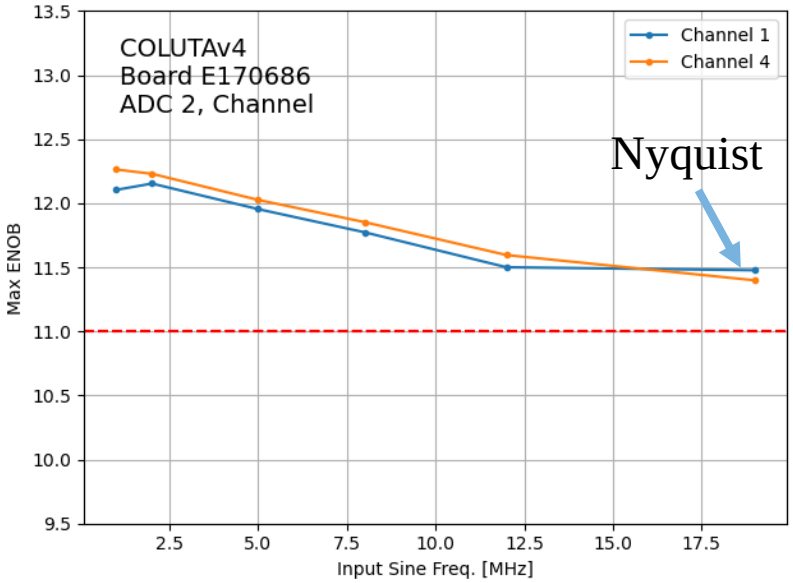
- Pedestal measurements on chs. 1, 4
- ~1.2 ADC counts RMS of noise
- Featureless pedestal FFTs

Sine Wave Performance

- Assess performance by varying amplitude and frequency of input sine signal
  - Input sine provided by AWG connected directly to board with filter and/or attenuators
  - FFTs at roughly full-scale show ~12b ENOB (spec. >11b @ 8MHz)
  - Performance across frequency range exceeds spec. up to Nyquist







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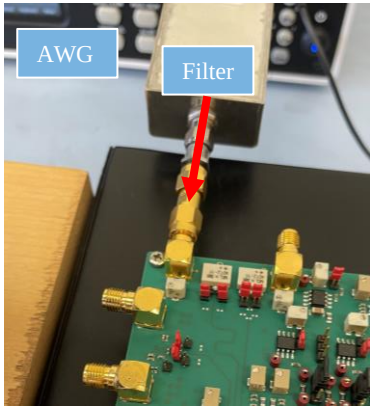
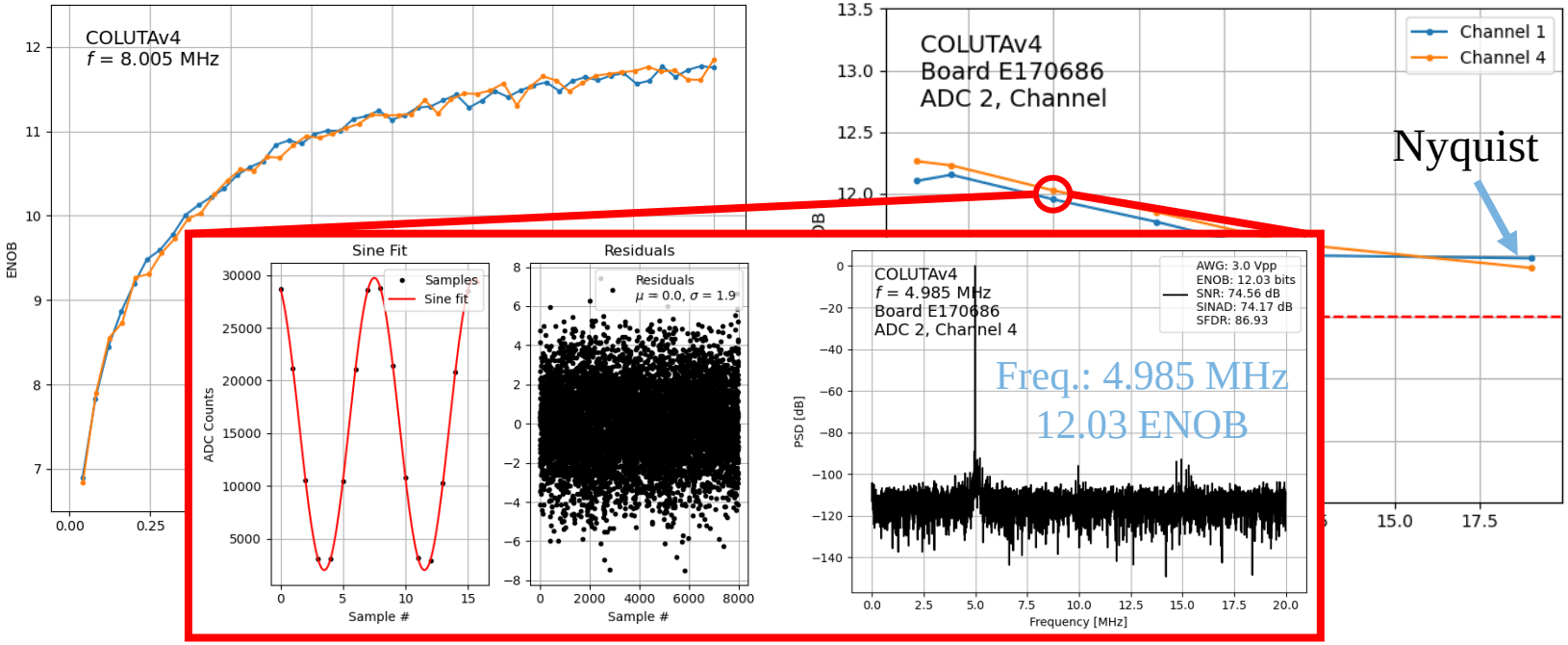




DNL & INL Measurements

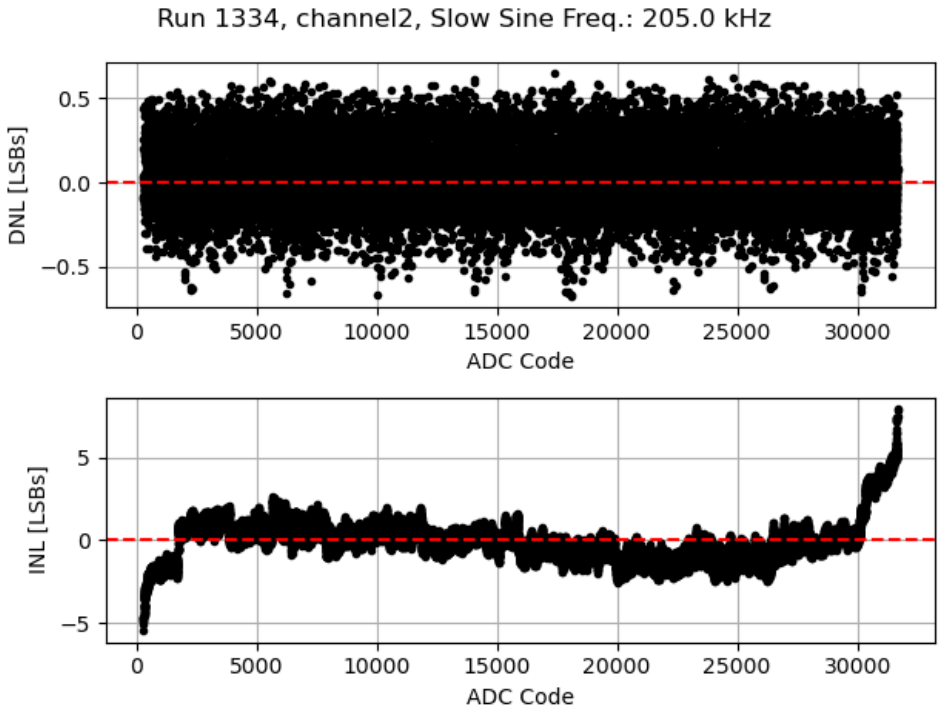
- Slow sine input (~200 kHz) used to test for nonlinearity
- DNL computed from linearized transition voltages V_j and INL from linear fit*
  - Results (shown in 15b LSBs) show no missing codes

$$\mathrm{DNL}_j = \frac{V_{j+1} - V_j}{1\ \mathrm{LSB}} - 1$$

$-0.67/+0.65$ 15b LSB
$(-0.07/+0.08$ 12b LSBs)

$$\mathrm{INL}_j = \frac{V_j - V_{\mathrm{fit},j}}{1\ \mathrm{LSB}}$$

$-5.51/+7.98$ 15b LSB
$(-0.69/+1.00$ 12b LSBs)

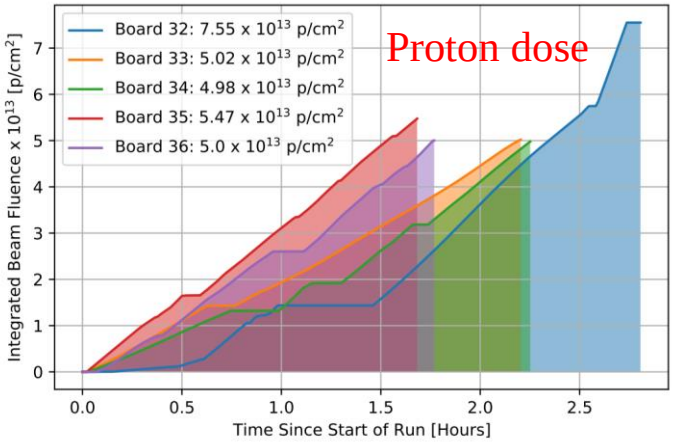


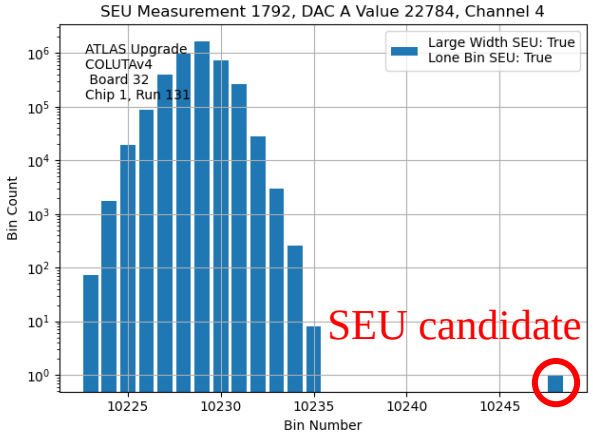
- DNL $-0.07/+0.08$ (spec. $-1.0/+1.0$ 12b LSBs), INL <0.03% (spec. <0.1%)

*See backup

Radiation Tolerance

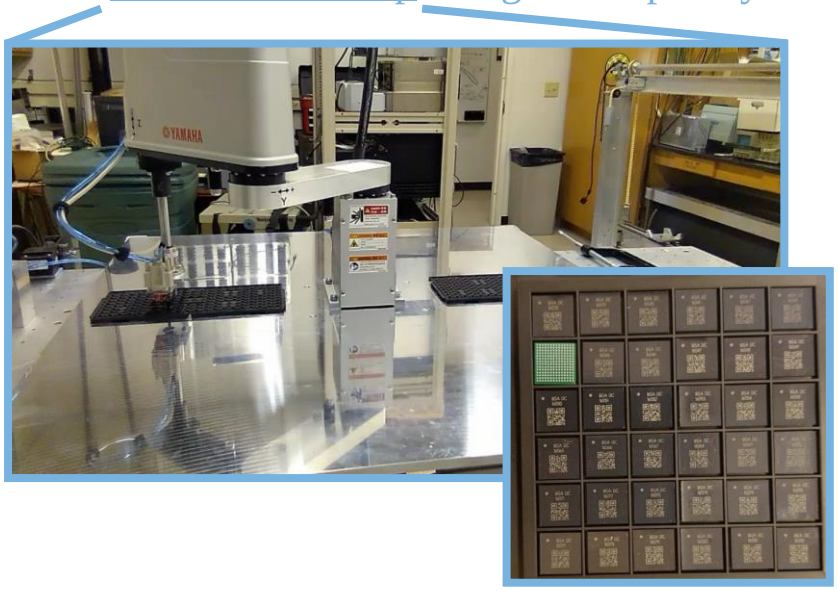
- Radiation testing performed at Mass General Hospital (Boston) proton treatment facility
- **Irradiated five chips beyond the spec. (~5×10^{13} p/cm^2)**
  - No performance degradation post-irradiation (assessed w/ sine wave performance)
  - General chip health (current draw, temperature) stable through irradiation
  - Preliminary count of triple redundant configuration corruptions 3 orders of magnitude better than previous chip version (CV3)
    - Due to moving triple redundant DFFs storing configuration bits further apart
  - Measurement of radiation induced effects (i.e. single event upsets (SEUs)) ongoing
    - Assessed by connecting onboard DAC to CV4 input + sweeping DAC over analog input range and histogramming in FPGA

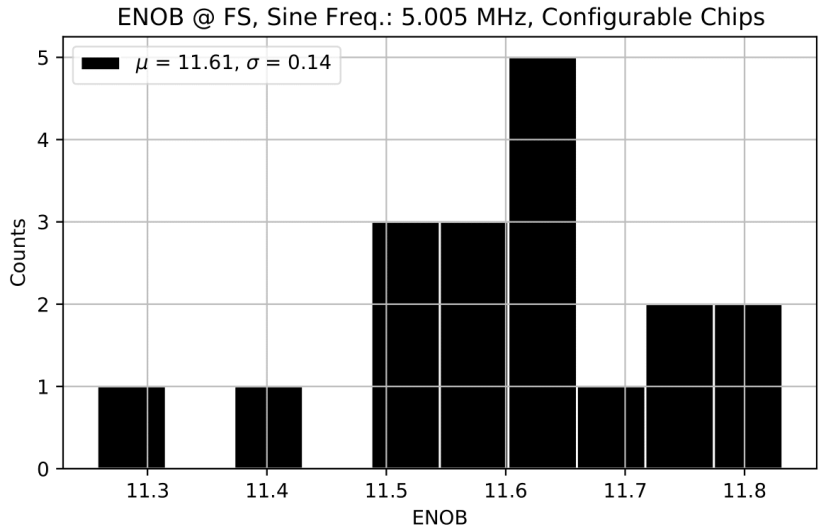




QA/QC

- ❖ Thus far produced 20 packaged chips in QFN100, produced in MPW → 18/20 chips functional
  - Investigating remaining two, may be possible to recover
- ❖ Functional chips show good performance out-of-the-box
  - E.g. sine performance on channel 1 at ~full-scale >11b ENOB across all functional chips
- ❖ **Final design review scheduled for Oct. 7**
  - Launch pre-production engineering run, followed by production of 80k chips
  - Future batches will be in BGA packaging
  - Robotic test setup being developed by UT Austin & Saclay for mass testing





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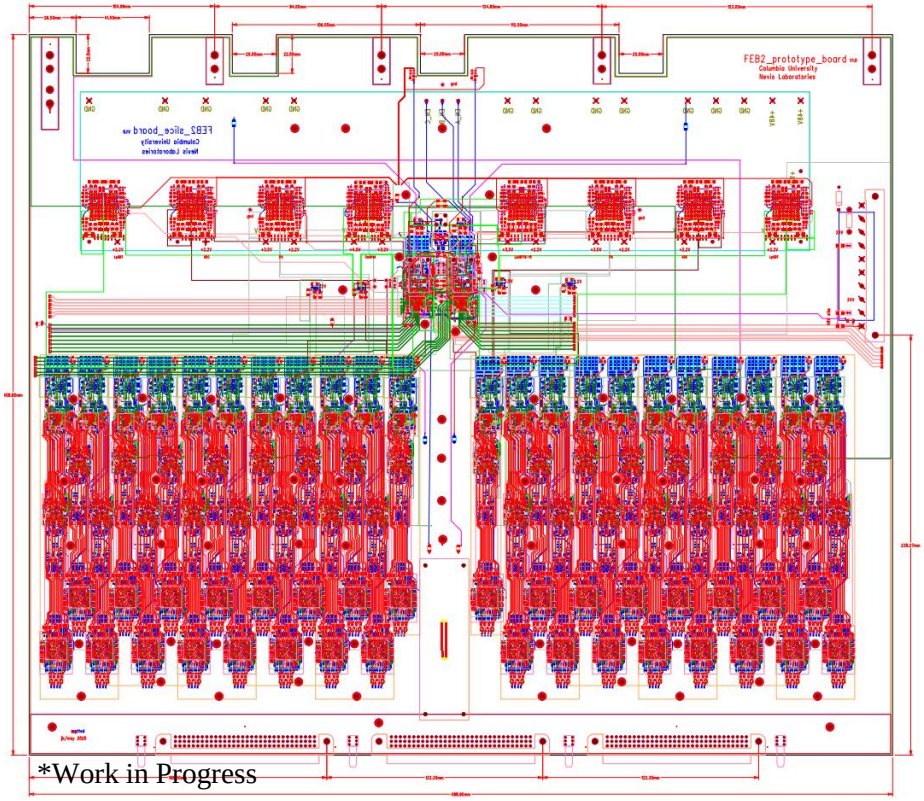
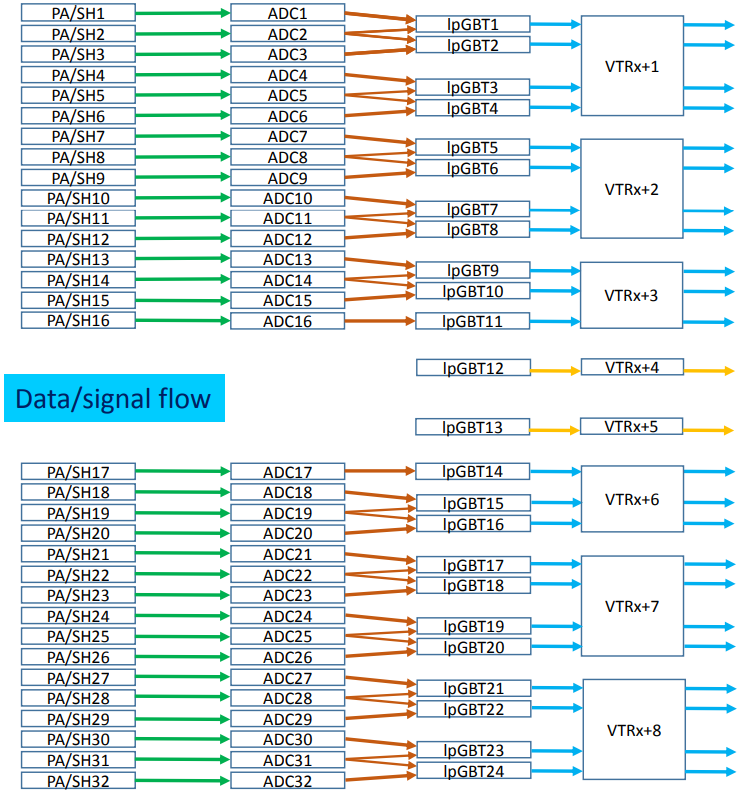
FEB2 Overview (1)

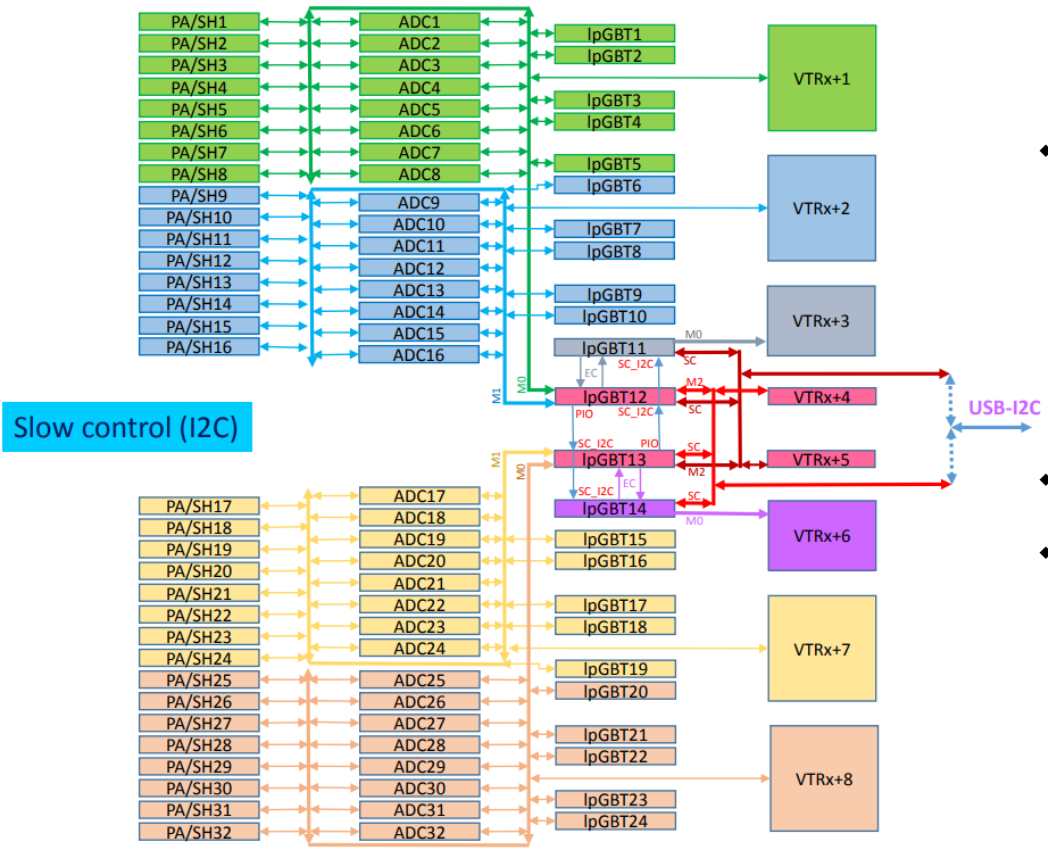
- FEB2 boards will provide the front-end readout of both gains of the LAr calorimeter
  - 128 channels/board, with a total of 1524 boards for calorimeter
  - Readout chain composed of PA/S (×32) → ADC (×32) → lpGBT (×24)→ VTRx+ (×8)



*Work in Progress



FEB2 Overview (2)

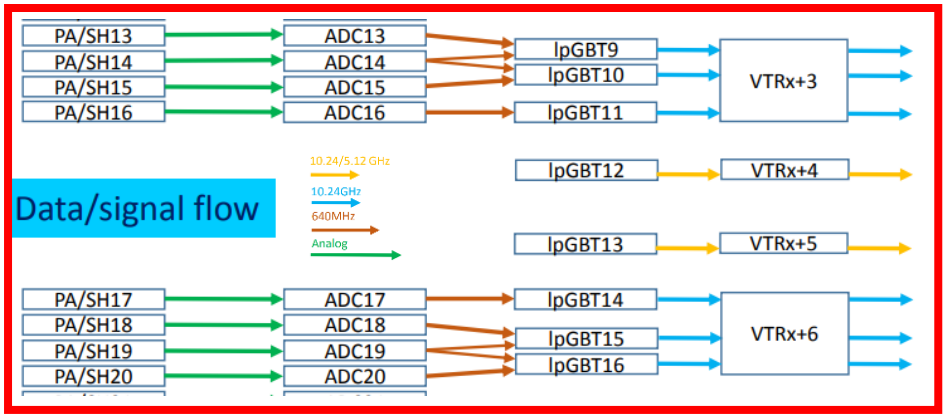


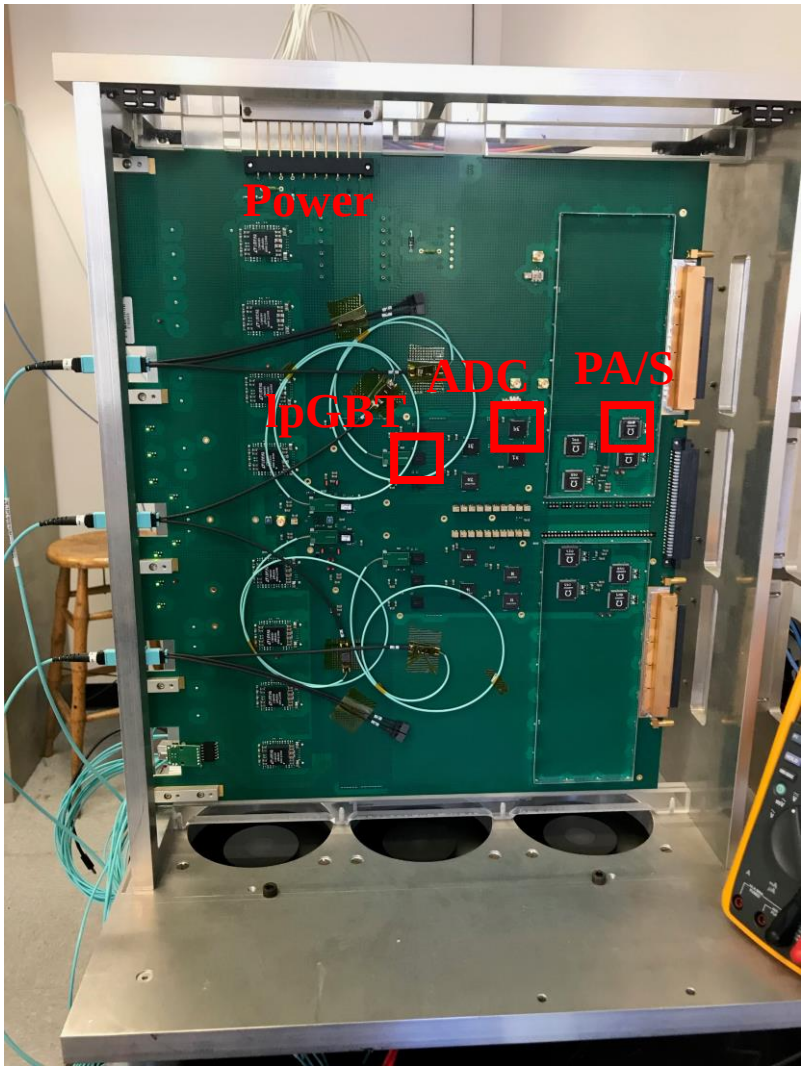
- Redundant bi-directional control/monitoring provided using lpGBTs 12 & 13
  - Control lpGBTs provide phase programmable 40MHz clock
  - Operational phases w.r.t. I2C clock found through clock parameter scan procedure
- VTRx+ implemented for data + control links
- DC-DC converters bring down 48V input, while LDOs provide final power rails at 1.2V and 2.5V (PA/S & VTRx+)

FEB2 Pre-Prototype: Slice Testboard

- ❖ Integration test of FEB2 components performed with pre-prototype FEB2 Slice Testboard
  - A “slice” of full FEB2 → same chip density + layout as final boards
  - 32 of final 128 channels implemented
- ✓ Validated I2C interface and redundant control
- ✓ Noise and pulse performance thoroughly assessed
  - Triangle LAr current pulses injected through two injector loads corresponding to 25Ω/50Ω input impedance settings of PA/S

Slice Testboard block diagram → 8 PA/S + ADCs + lpGBTs, 4 VTRx+





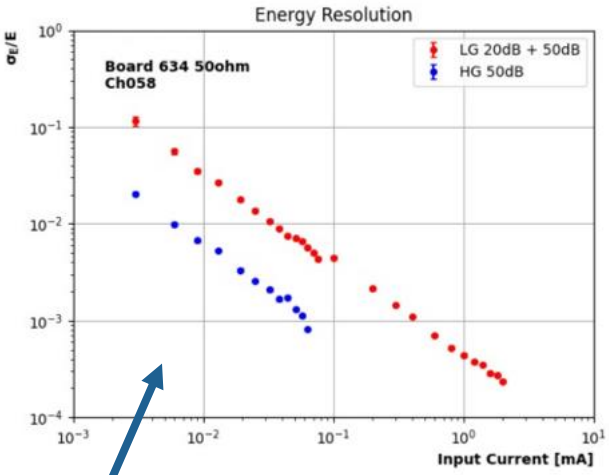
FEB2 Slice Testboard Performance

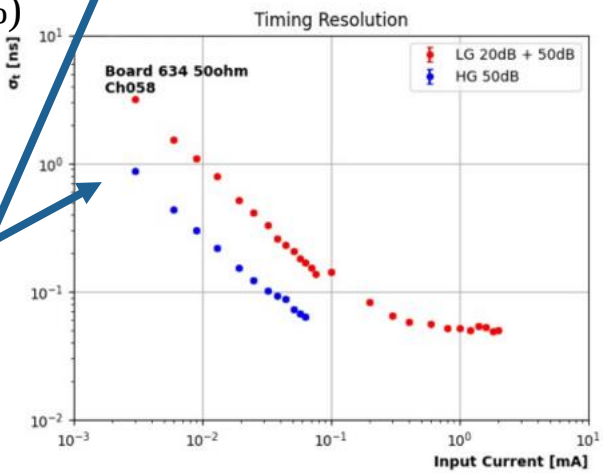
❖ **Noise performance** dominated by detector capacitance + PA/S

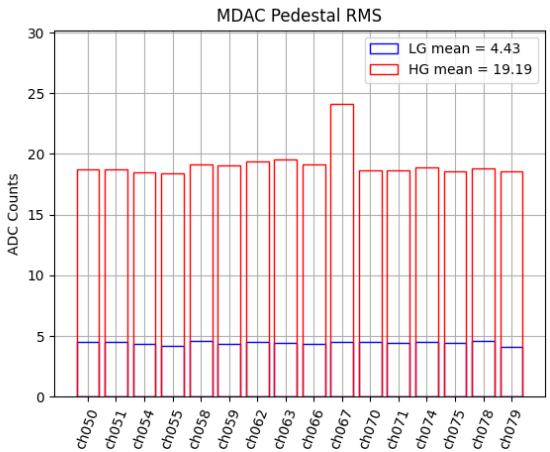
Setting	LG Noise [ADC]	HG Noise [ADC]	Hi/Lo Gain Ratio
25Ω	4.0	19.2	25.6
50Ω	4.0	35.65	37.4

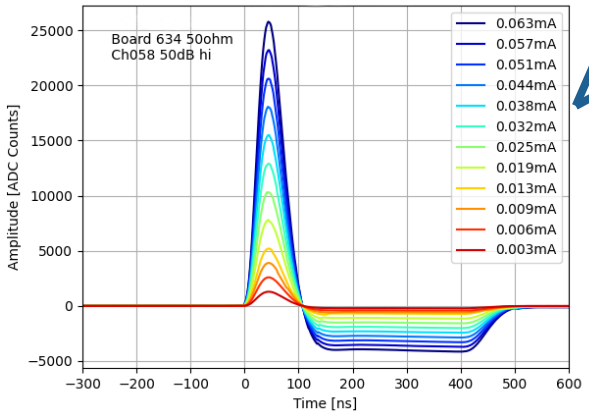
❖ **Pulse performance** determined from pulsing board at amplitudes spanning the dynamic range

- Apply digital filters to pulse measurements for energy/timing
  - **Energy resolution ~.02%** for large pulses (spec. <0.25%)
  - **Timing resolution ~ 50 ps** (dominated by ext. system)



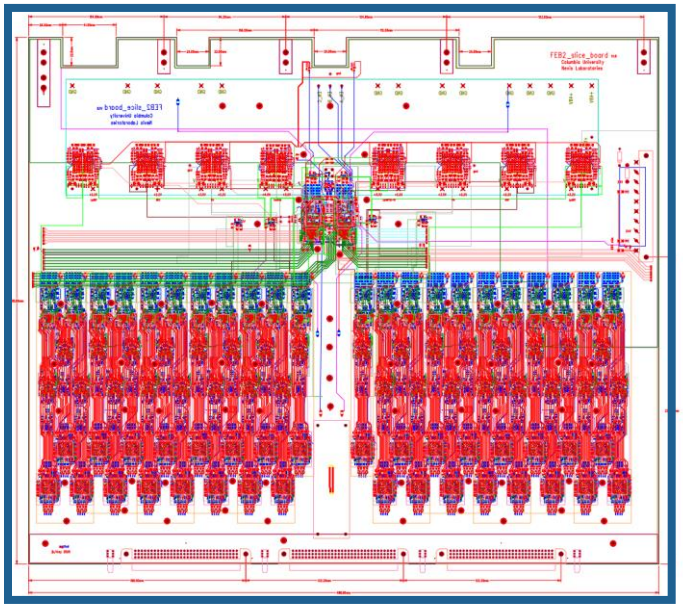






FEB2 Prototype Timeline

- **Integration test of FEB2 through the Slice Testboard meets and exceeds specs.**
- Next step in testing is the FEB2 prototype
  - Full 128 channels
  - ASICs to be packaged in BGA (instead of current QFP/QFN)
  - Updating to latest prototypes of PA/S, ADC ASICs



- Timeline
  - **Present:** Finalizing FEB2 prototype design
    - Rad-tolerant power testing at INFN Milano
    - Characterizing integration between latest PA/S and ADC ASICs
    - Finalize selection of rad-hard LDOs
  - **Nov. 2022:** FEB2 preliminary design review
  - **Early 2023:** fabrication of 2 FEB2 prototype boards with “almost final” design + ASICs
  - **2023:** Front-end system crate test with 14 FEB2 boards (1% of full scale)
  - **2024-2026:** Full production of 1524 FEB2s

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Conclusions

- ❖ HL-LHC increase in luminosity and data volumes
  - Replacement of readout electronics for ATLAS LAr calorimeters
- ❖ Provided overview of the COLUTA LAr ADC
  - Currently in fourth and final prototype iteration
  - Characterized sine performance, nonlinearity, and radiation tolerance
    - Performance meets and exceeds specs. for HL-LHC
  - ➢ **CV4 is ready for final design review (Oct. 7) and pre-production**
- ❖ Provided overview of FEB2 design and integration testing with FEB2 Slice Testboard
  - Validated I2C interface, redundant control structure, noise and pulse performance
  - ➢ **Currently finalizing design of FEB2 prototype for preliminary design review (Nov.)**

THANK YOU!

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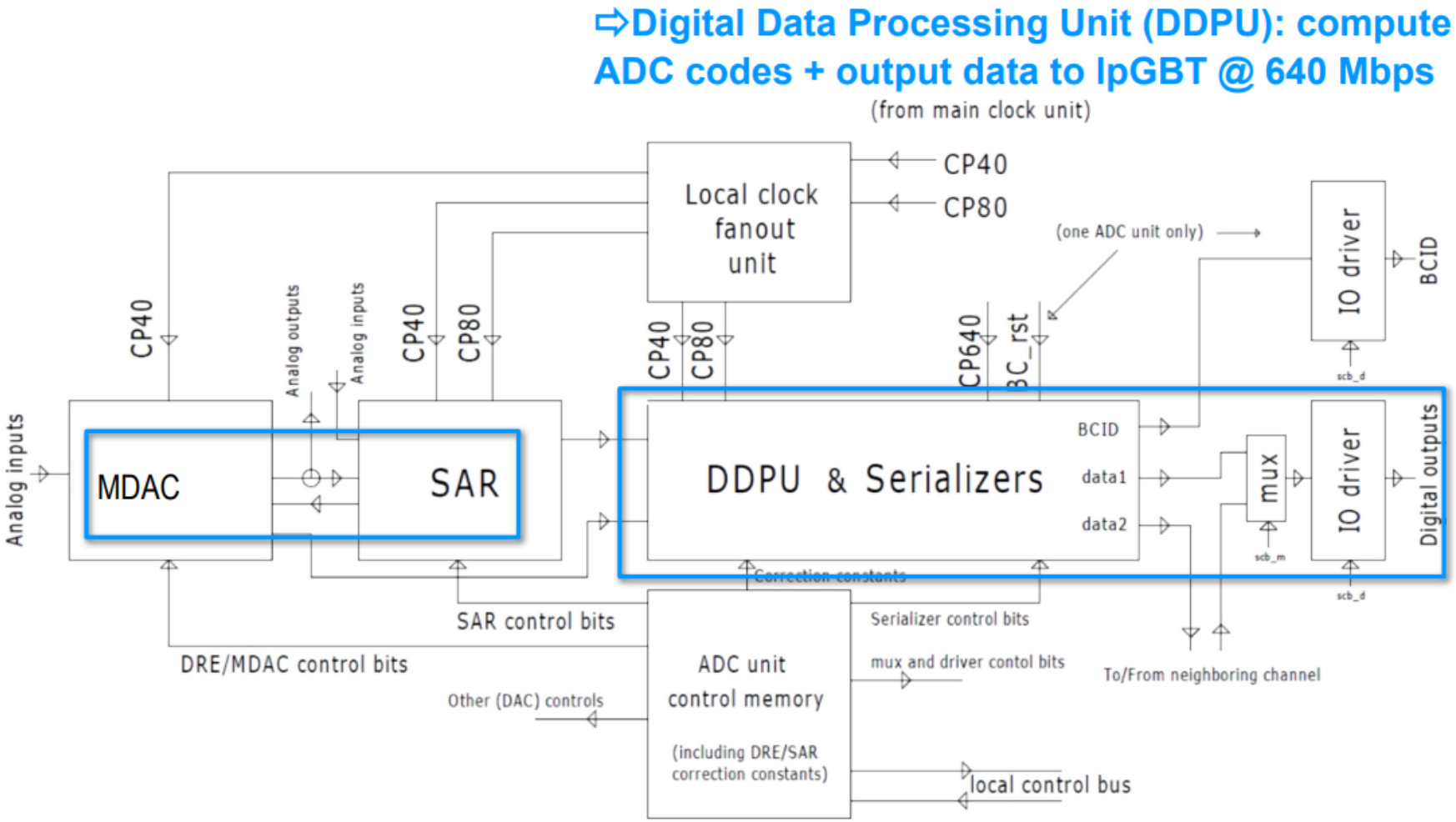
BACKUP

COLUTAv4 Channel (x8) Block Diagram

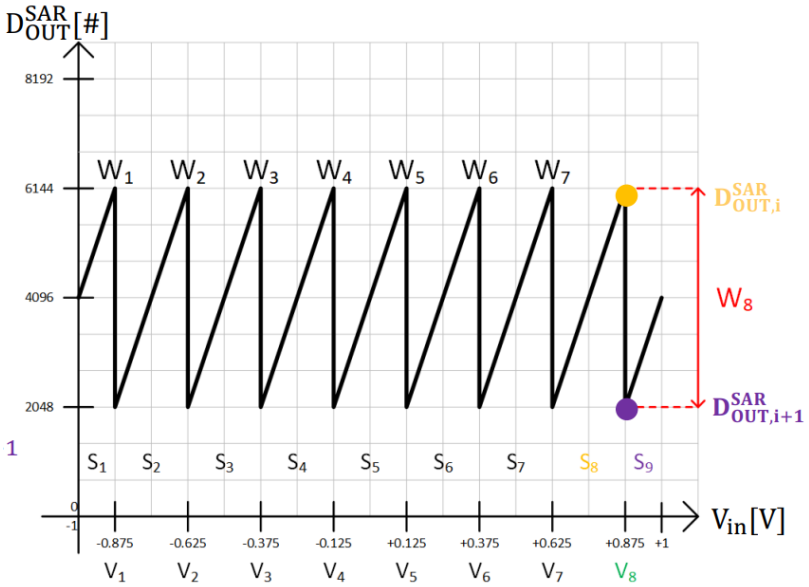


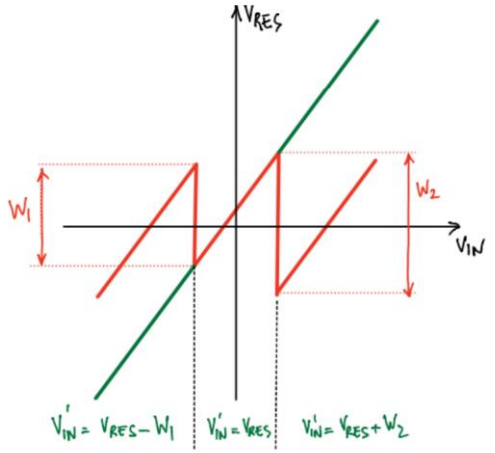
MDAC Calibration Process

- Procedure
  1) Assert V_i
  2) Force S_i
  3) Measure $D_{\mathrm{OUT},i}^{\mathrm{SAR}}$
  4) Force S_{i+1}
  5) Measure $D_{\mathrm{OUT},i+1}^{\mathrm{SAR}}$
  6) Calculate $W_i = D_{\mathrm{OUT},i}^{\mathrm{SAR}} - D_{\mathrm{OUT},i+1}^{\mathrm{SAR}}$
  7) Repeat for $i = 1$ to 8
- DDPU uses $W_1,\ldots,W_8$ to "stitch together" subranges and create a linear transfer function

$$D_{\mathrm{out}}^{\mathrm{MDAC+SAR}} = D_{\mathrm{OUT}}^{\mathrm{SAR}} - 4096 + \sum_{i=1}^{8} W_i \cdot b_i$$

- All calibration circuitry is on-chip
- MDAC calibration is done after SAR calibration



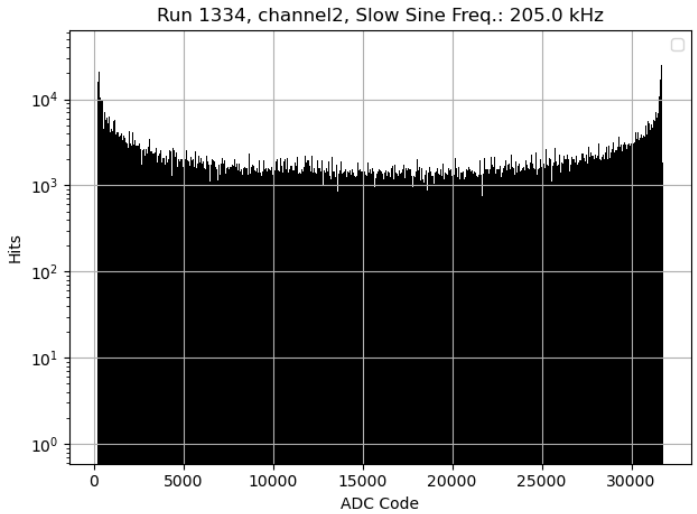


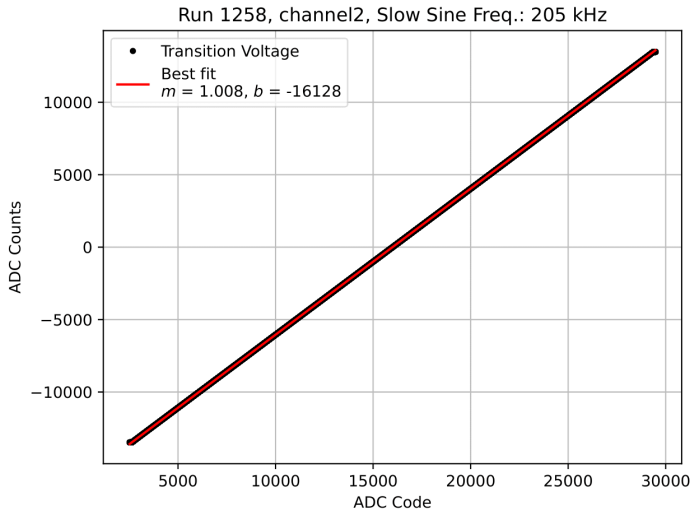
Slow Sine DNL/INL Methodology

❖ Derive transition voltages (method outlined in [this document])

$$V_j = -A\cos\left(\frac{\pi}{M}\sum_{k=0}^{j} H_k\right)$$

A = amplitude in ADC counts
M = total number of samples
H_k = contents of kth sine histogram bin

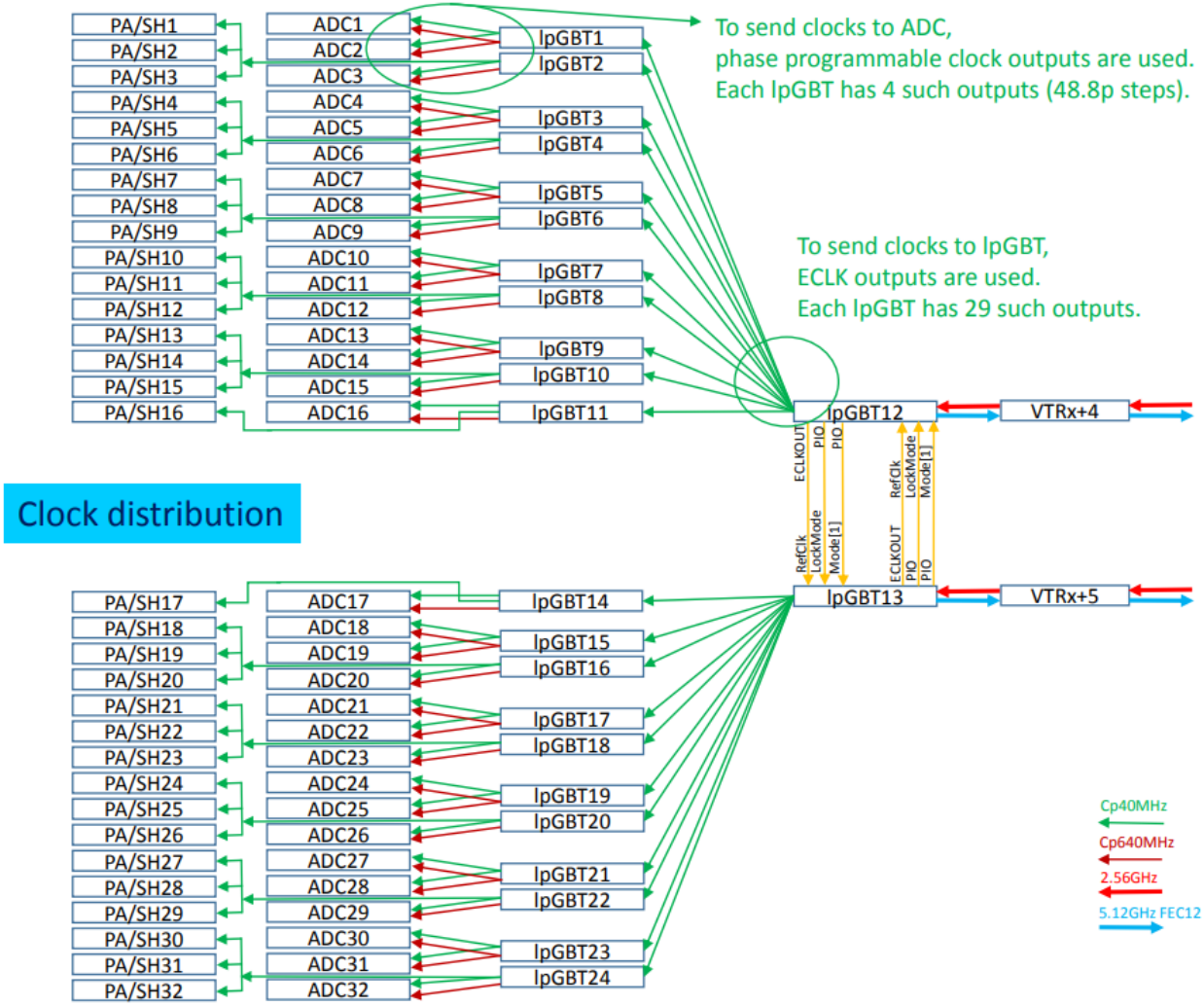




❖ Transition voltages takes sine histogram (left) and linearizes it (right)

❖ Use to define $\mathrm{DNL}_j = \frac{V_{j+1} - V_j}{1\ \mathrm{LSB}} - 1$ and $\mathrm{INL}_j = \frac{V_j - V_{\mathrm{fit},j}}{1\ \mathrm{LSB}}$

FEB2 Clock Distribution

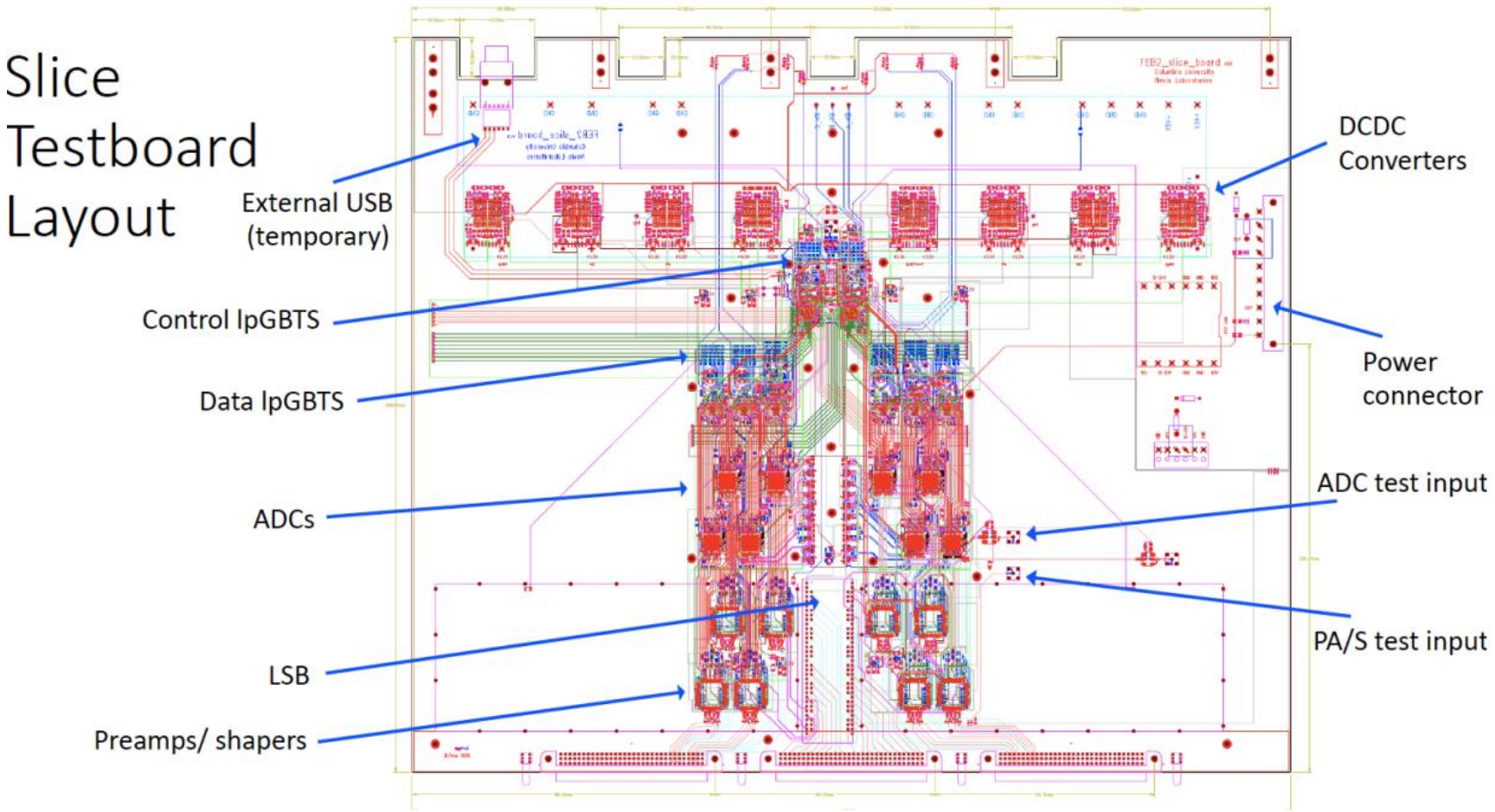


LDOs

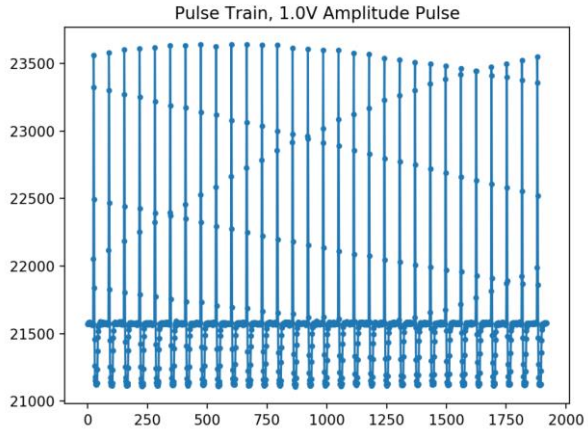
- To achieve analog performance goals, FEB2 needs “clean power” at 1.2V and 2.5V (PA/S & VRTX+)
  - FEB2 on-board powering scheme uses DC-DC convertors to get from 48 V input down to “close to” the final voltages, followed by LDOs for final power rails
  - LT3080 (on Slice Testboard) showed hard failures during radiation testing

1. Solution for 1.2 V: CMS rad-hard LDO for developed for HGCAL (max Vout = 1.5 V; does not work for 2.5 V ASICs)
   - A few rounds of pre-prototypes have been successfully produced and tested, meeting CMS performance specs
   - New FEB2 power scheme would require up to 48 CMS LDOs per board (updated power budget = 101 W/board)
   - Need to pin down possible remaining concern about single-effect transients (SET) via additional proton test
   - Testing possible with Analog Testboard, finalizing mezzanine design
2. Solution for 2.5 V: reuse ST LHC4913 from original construction
   - Need ~3500 in total: possibility to assemble through stock of spare FEB parts, plus other spares, plus recovering LDOs from spare FEB boards at CERN
   - Finalizing inventory of available devices

Slice Testboard Layout

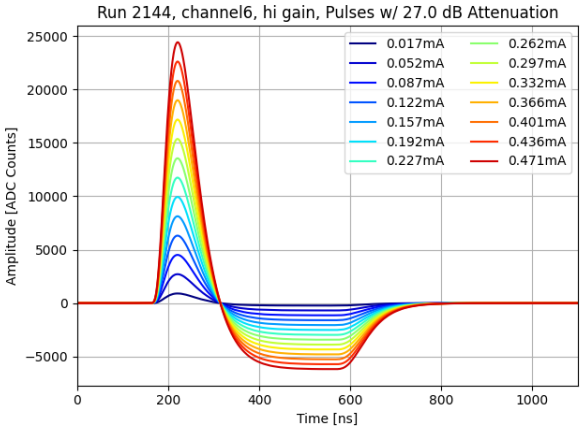


Pulse Analysis Overview

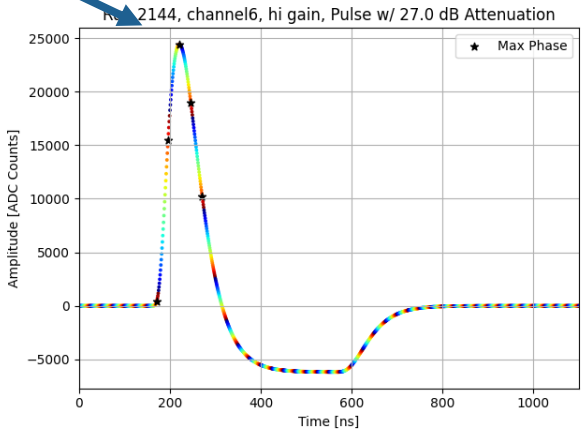


- AWG sends a pulse train of known amplitude to ADC chip, sampled at 30 different phases

- Pulse train is interleaved to create a fine resolution pulse



- Samples from phase of smooth pulse (and its derivative) containing peak are used to compute OFCs

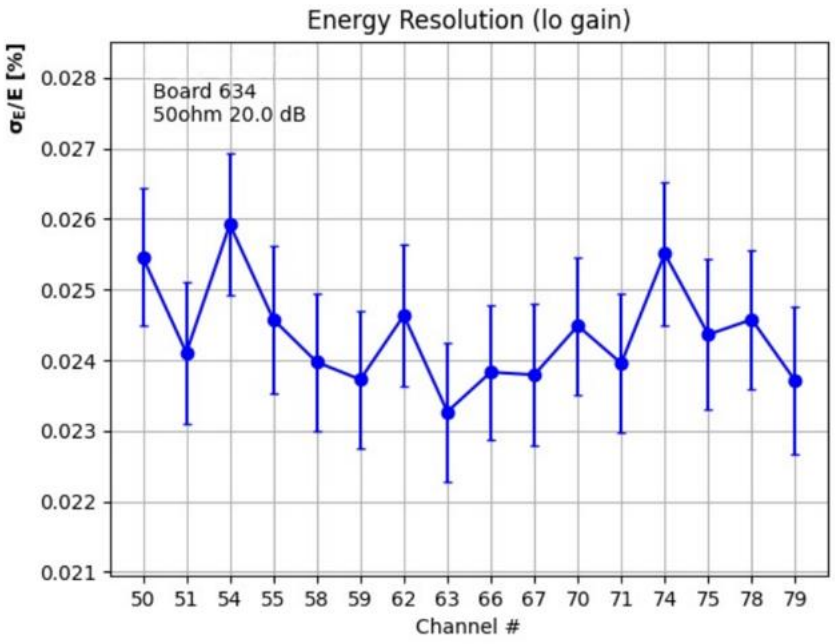


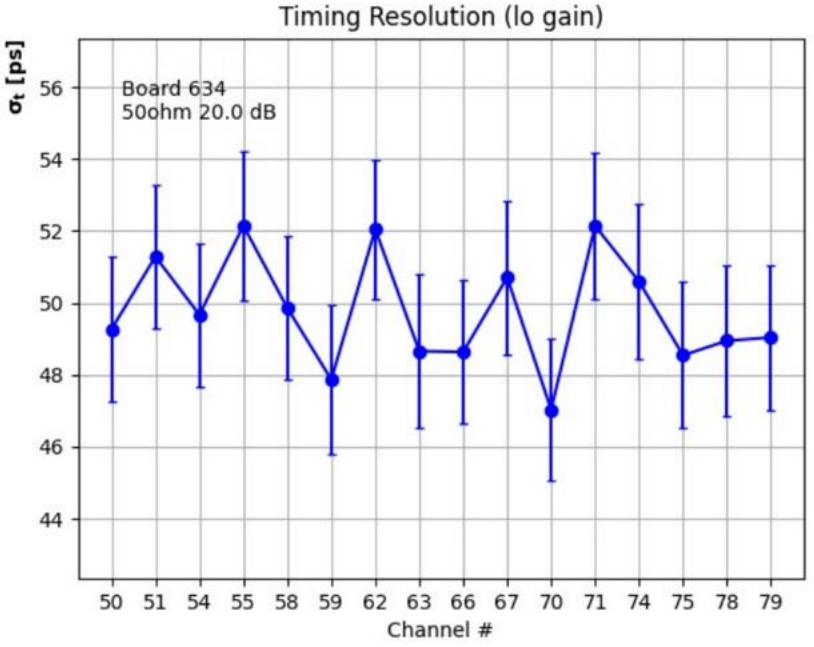
- OFCs used to compute energy and timing (see Cleland & Stern)
- Where a_i, b_i are OFCs:

$$E = \sum_{i=1}^{n} a_i s_i \quad \text{and} \quad E \times t = \sum_{i=1}^{n} b_i s_i$$

Multichannel Performance of Slice Testboard

- Energy resolution of ~0.02% and timing resolution of ~50 ps consistent across Slice Testboard channels for both 25 and 50Ω modes (here 50Ω is shown)





Integration of ALFE2 with COLUTA

- ALFE2 PA/S → replaces LAUROC (currently in Slice Testboard)
  - Integration with CV4 assessed on the CV4 Testboard
  - Pedestal noise up to ~2x better than CV3+LAUROC

Setting	CV3 + LAUROC LG Noise [ADC]	CV3 + LAUROC HG Noise [ADC]	CV4 + ALFE2 LG Noise [ADC]	CV4 + ALFE2 HG Noise [ADC]
25Ω	4.0	19.2	2.57	14.02
50Ω	4.0	35.65	2.28	18.84

  - Energy resolution down to ~0.02% for largest pulses
    - On par with Slice Testboard results and well within specs