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The COLUTA ADC ASIC in the ATLAS HL-LHC Liquid Argon Calorimeter Readout

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The upgraded high-luminosity Large Hadron Collider (HL-LHC) requires a new radiation tolerant ATLAS Liquid Argon Calorimeter readout operating at 40MHz with 16-bit dynamic range. The COLUTA is a 65nm CMOS custom 8-channel 15-bit 40 MSPS ADC ASIC developed for this application, coupling a 3.5-bit Multiplying-DAC (MDAC) stage to a successive approximation register (SAR) ADC. A Digital Data Processing Unit (DDPU) outputs sample data continuously via 640 Mbps serial LVDS. Prototype COLUTA performance above specification at >11.5 ENOB for relevant frequencies and "Slice Testboard"integration test results will be presented.

Summary (500 words)

To meet the physics challenges in the difficult experimental environment of the upgraded High-Luminosity Large Hadron Collider (HL-LHC), with up to 200 simultaneous collisions taking place each bunch crossing at 40 MHz, the ATLAS detector requires development of new readout electronics for its Liquid Argon (LAr) calorimeter. The frontend readout of the new LAr HLLHC electronics system will be implemented on a "Front-End Board 2"(FEB2), with each board handling 128 channels and integrating electronic components that receive the input calorimeter signals which have up to 16-bit dynamic range, apply amplification and analog shaping as well as splitting them into two overlapping linear gain scales, followed by sampling and digitizing both gains at 40 MSPS, and then serializing the digital data at 10 Gbps and transmitting them off detector via multiple optical links. Since the FEB2 boards will be mounted on the detector cryostats, they must tolerate significant radiation levels, greatly limiting the applicability of commercial devices. Instead, the main functionality has been developed in a set of custom ASICs, including a preamplifier/shaper, an ADC, and a serializer/transceiver.

The COLUTA is a custom 8-channel 15-bit 40 MSPS ADC ASIC developed in 65nm CMOS for this application, with an architecture that couples a 3.5-bit Multiplying-DAC (MDAC) stage to a successive approximation register (SAR) ADC back-end. Each channel also includes an on-chip Digital Data Processing Unit (DDPU) that applies the MDAC and SAR calibration constants and formats the output data. Sampled signal data and frame information are continuously output via 640 Mbps serial LVDS links to CERN Low Power Gigabit Transceiver (lpGBT) ASICs. Prototype versions of the COLUTA demonstrate sampling performance above specification at >11.5 ENOB in the relevant frequency range. The development and performance of COLUTA prototypes will be presented, along with results of preliminary integration tests in the "Slice Testboard"developed as a 32-channel pre-prototype of the final FEB2.

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