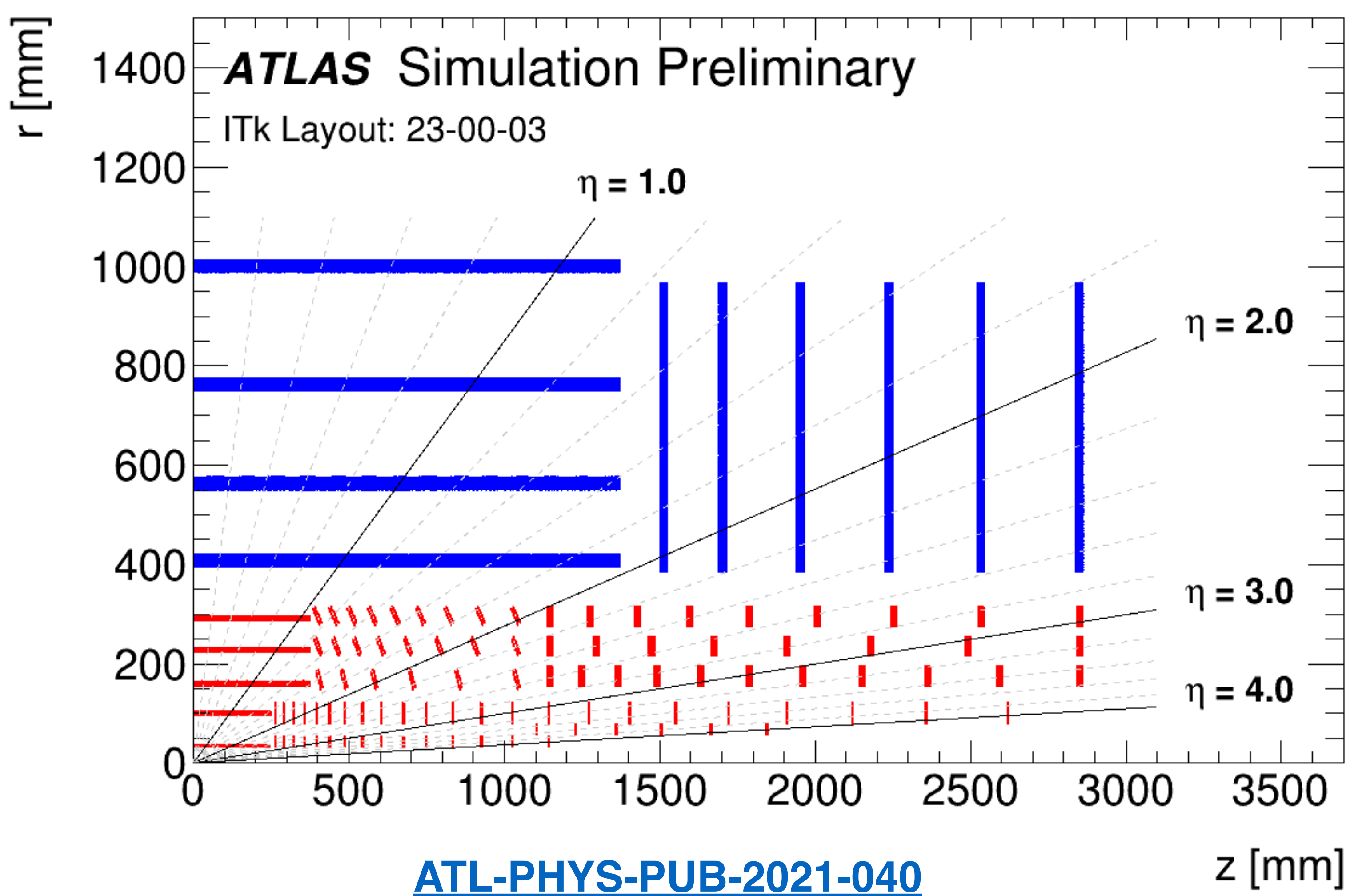
Simulated verification of ASIC functionality & radiation tolerance for HL-LHC ATLAS ITk Strip detector

Jeff Dandoy
University of Pennsylvania
On behalf of the ATLAS ITk Collaboration

Topical Workshop on Electronics for Particle Physics
20 Sept. 2022

ATLAS **I**nner **T**rac**k**er for HL-LHC

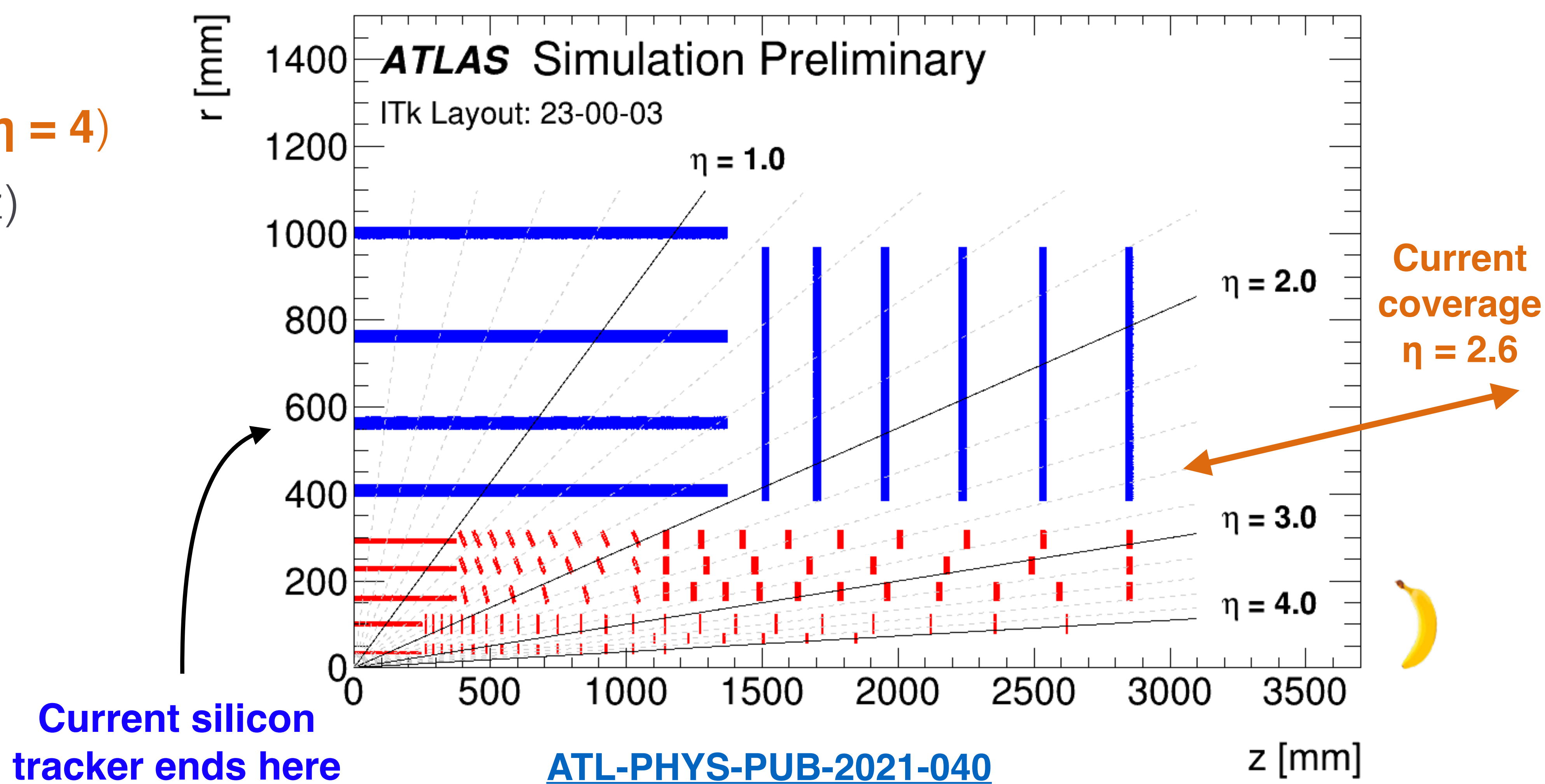
- ITk will replace current ATLAS Inner Detector for HL-LHC (installation in ~2027)
  - Track charged particles in busy environment of **~200 simultaneous collisions**
  - Operate for **>10 years** to collect 10x more data (4000 fb^{-1})
  - Survive in high-radiation environment, up to ~**1000** MRad (**inner**) or **50** MRad (**outer**)



ATL-PHYS-PUB-2021-040

ATLAS Inner Tracker for HL-LHC

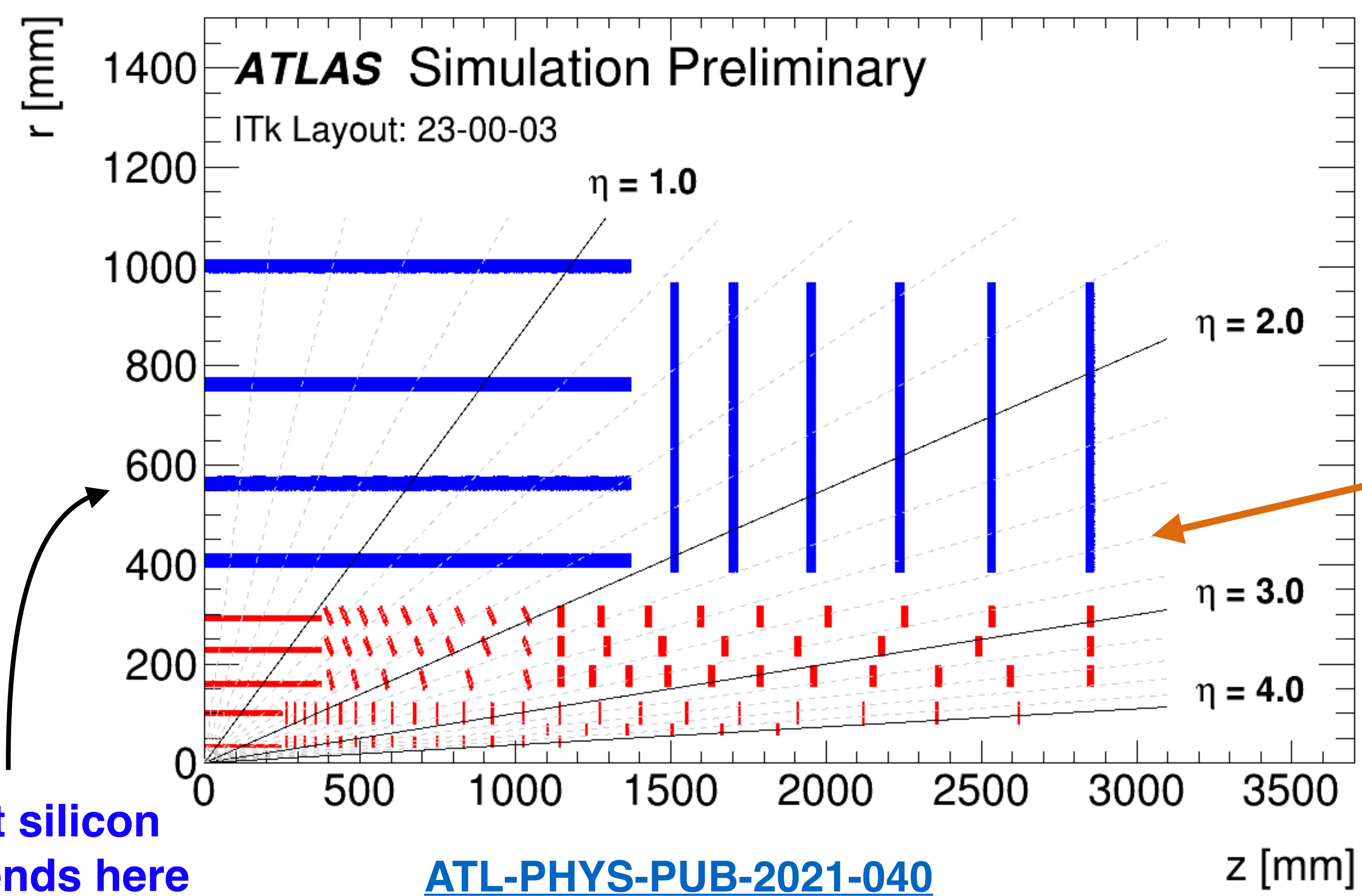
- ITk will replace current ATLAS Inner Detector for HL-LHC (installation in ~2027)
  - Track charged particles in busy environment of **~200 simultaneous collisions**
  - Operate for **>10 years** to collect 10x more data (4000 fb^{-1})
  - Survive in high-radiation environment, up to ~**1000** MRad (**inner**) or **50** MRad (**outer**)
- **Upgrading to all-silicon tracker**:
  - **Larger radius** (1 m)
  - **Finer segmentation** (50-75 μm)
  - **Coverage expanded (η = 4)**
  - **Faster readout** (1 MHz)



ATL-PHYS-PUB-2021-040

ATLAS **I**nner **T**rac**k**er for HL-LHC

- ITk will replace current ATLAS Inner Detector for HL-LHC (installation in ~2027)
  - Track charged particles in busy environment of **~200 simultaneous collisions**
  - Operate for **>10 years** to collect 10x more data (4000 fb^{-1})
  - Survive in high-radiation environment, up to ~**1000** MRad (**inner**) or **50** MRad (**outer**)
- **Upgrading to all-silicon tracker**:
  - **Larger radius** (1 m)
  - **Finer segmentation** (50-75 μm)
  - **Coverage expanded** (**η = 4**)
  - **Faster readout** (1 MHz)
- **Immense project** to design, verify, build, test, & operate
  - 165 m^2 of active silicon sensor
  - 60 million readout channels
  - **280,000 ASICs**



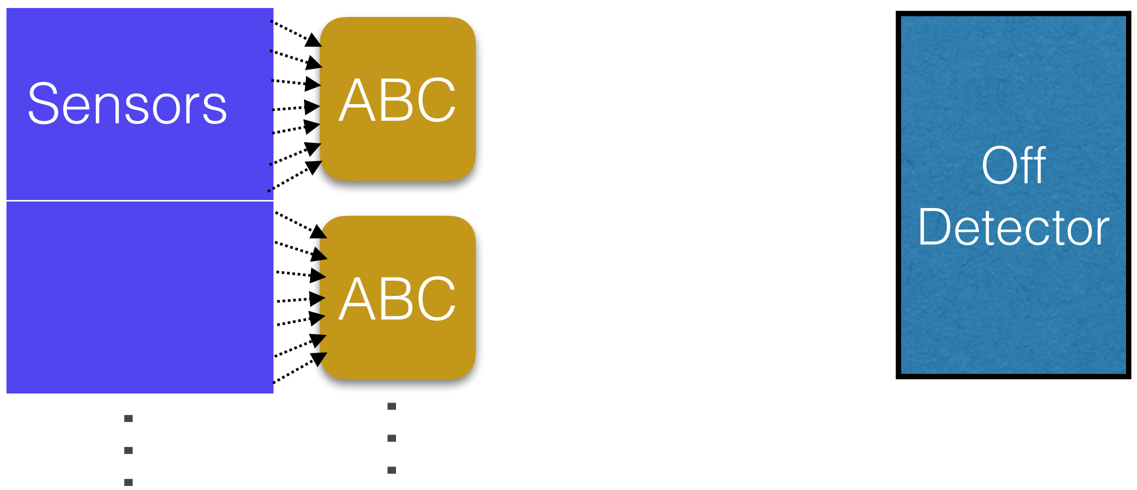
Current coverage η = 2.6

Current silicon tracker ends here

ATL-PHYS-PUB-2021-040

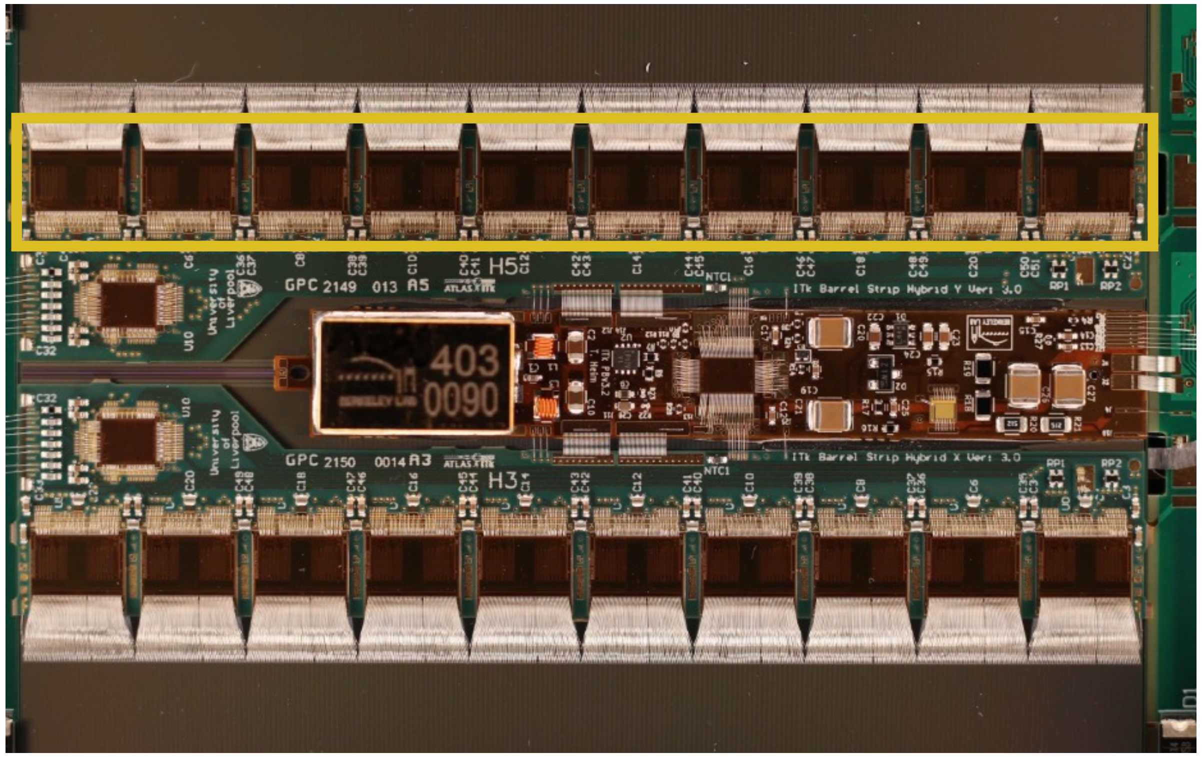
3 ASICs for ITk Strip detector

- Charged particles activate **strips of silicon sensors**
- **ABC** (ATLAS Binary Chip) reads 256 sensors, **digitize** & **compress data** into clusters



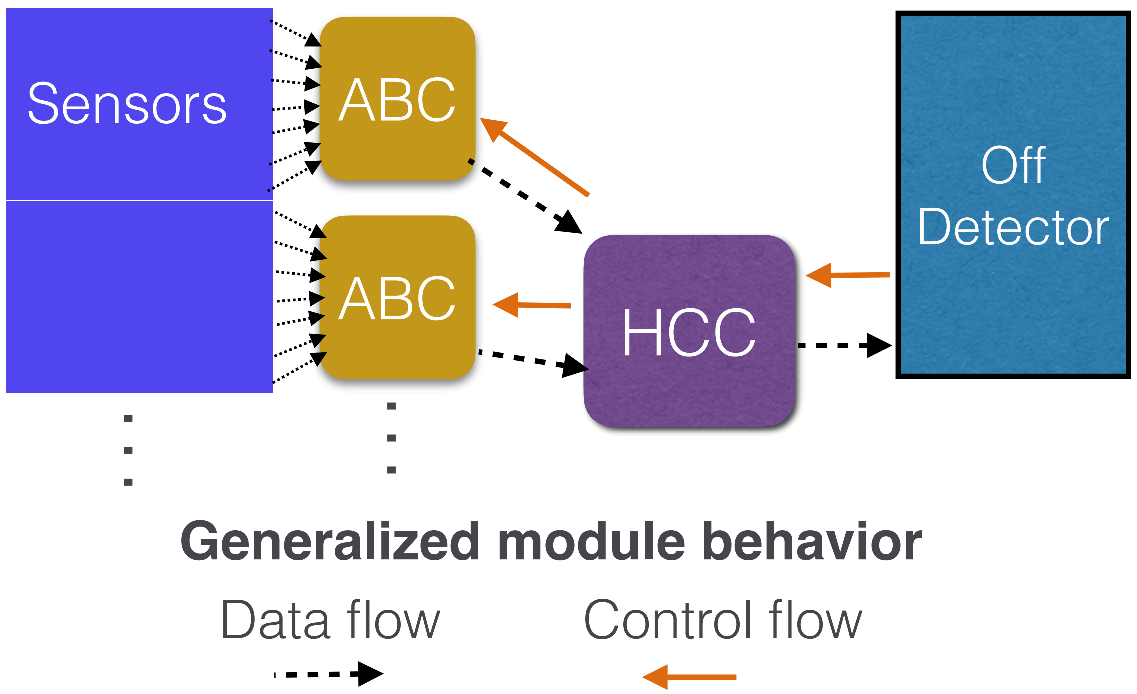
Generalized module behavior

Constructed module @ Brookhaven



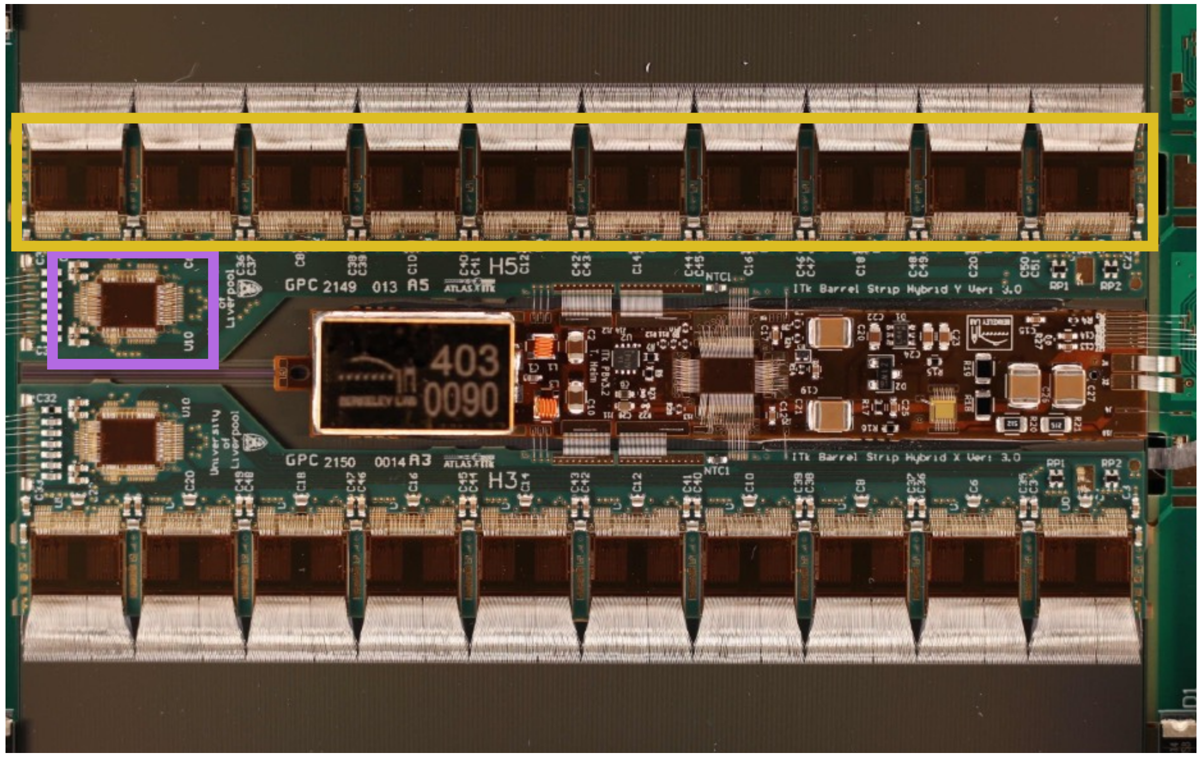
3 ASICs for ITk Strip detector

- Charged particles activate **strips of silicon sensors**
- **ABC** (ATLAS Binary Chip) reads 256 sensors, **digitize** & **compress data** into clusters
- **HCC** (Hybrid Controller Chip) **serializes data @ 640 MHz** for up to 11 ABCs, transmits commands & buffers trigger requests



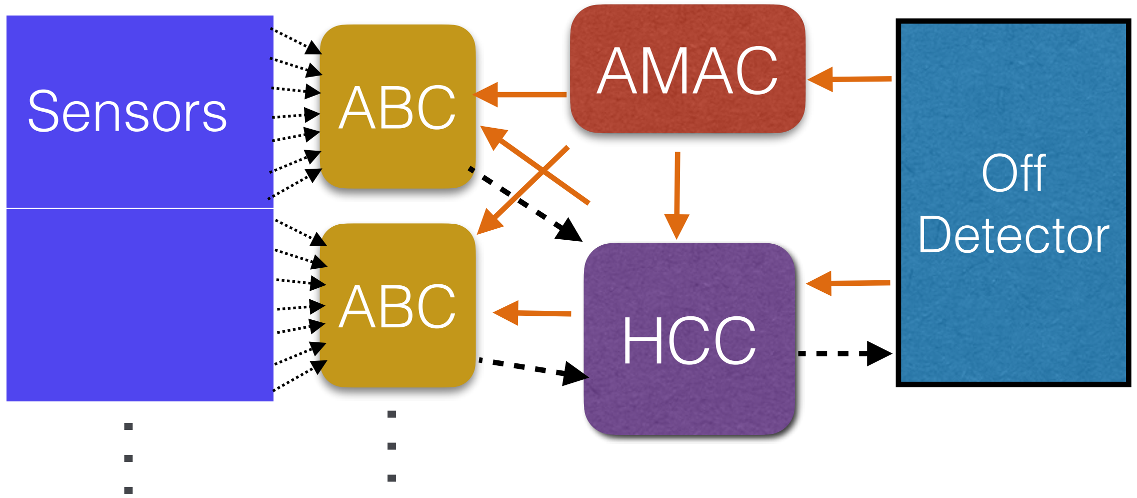
Generalized module behavior

Constructed module @ Brookhaven



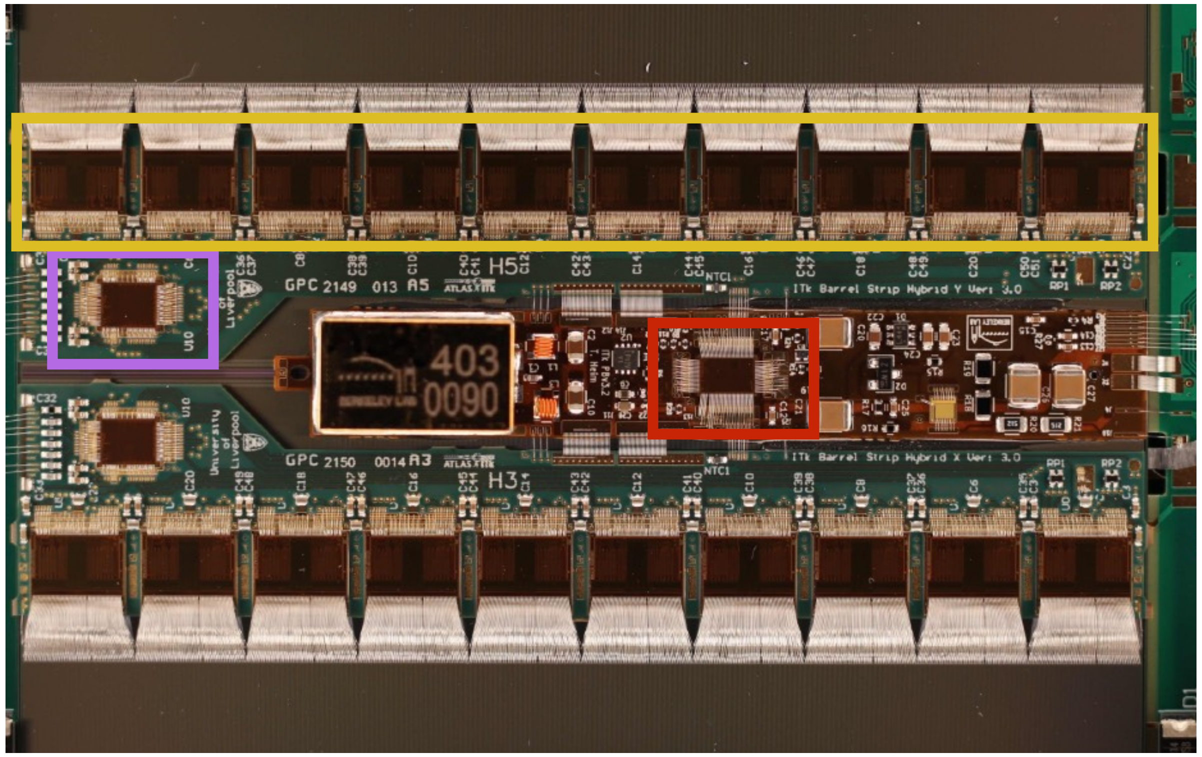
3 ASICs for ITk Strip detector

- Charged particles activate **strips of silicon sensors**
- **ABC** (ATLAS Binary Chip) reads 256 sensors, **digitize** & **compress data** into clusters
- **HCC** (Hybrid Controller Chip) **serializes data @ 640 MHz** for up to 11 ABCs, transmits commands & buffers trigger requests
- **AMAC** (Autonomous Monitoring And Control) - **monitors** voltages / currents / temperatures with **automatic system interrupts**
- Several design iterations for evolving needs (bandwidth, rad-hard), **final** "**StarV1**" versions now approved



Generalized module behavior

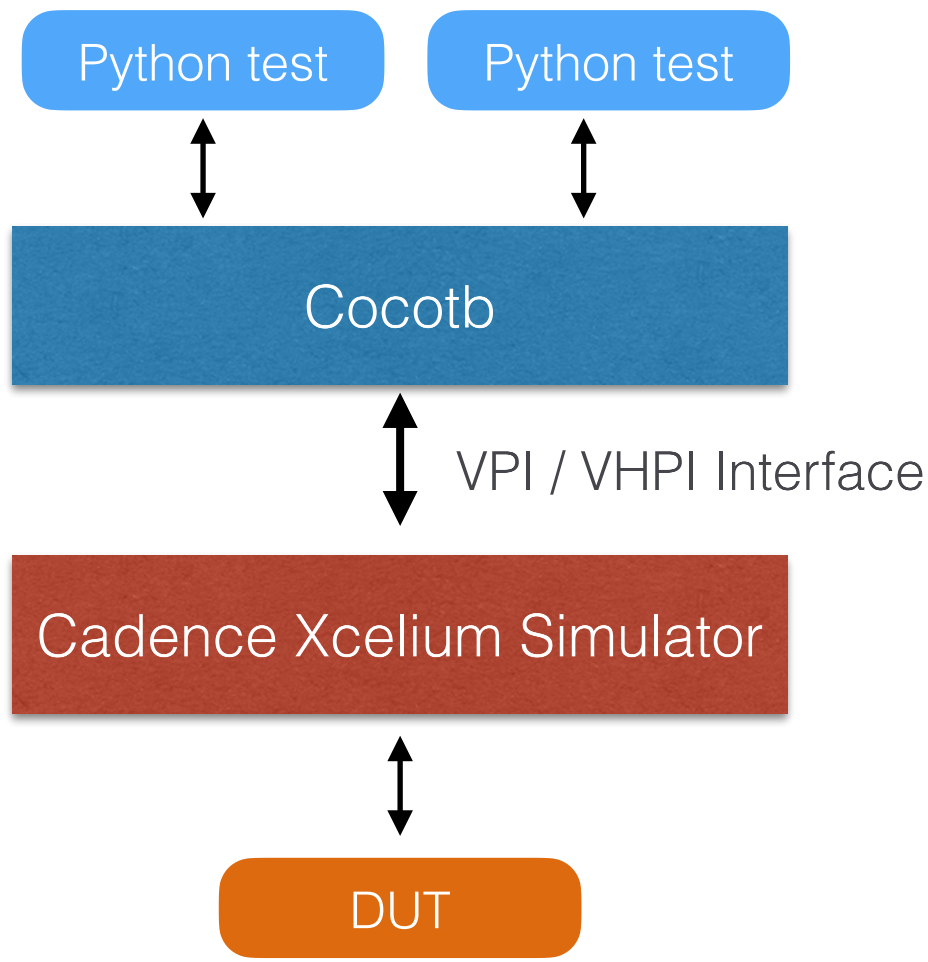
Constructed module @ Brookhaven



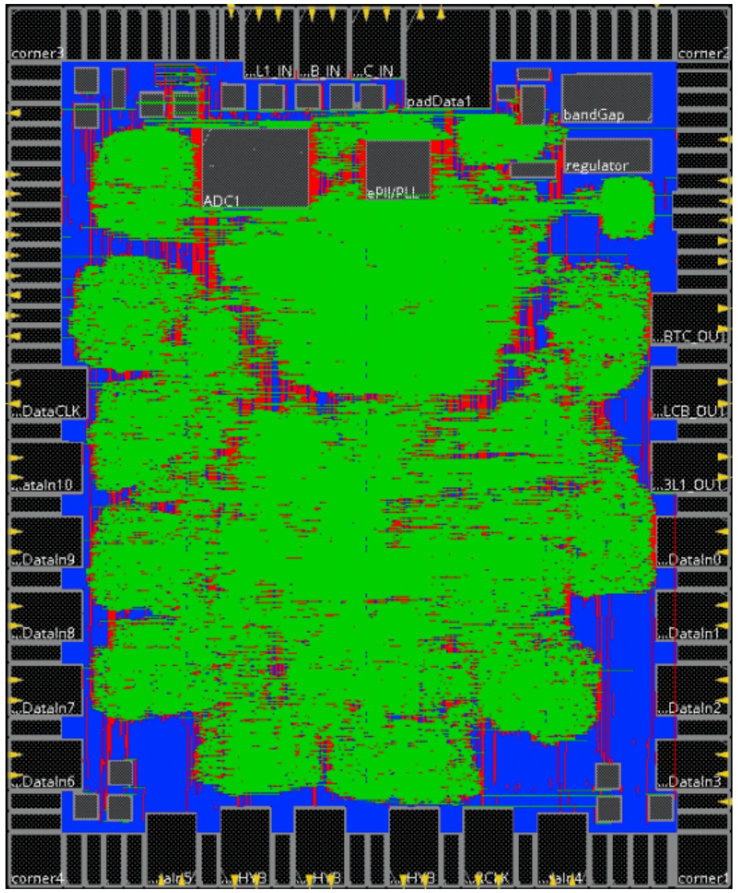
Simulation testbench

now supported by FOSSi Foundation

- Verify digital designs using python-based **cocotb**
  - **Co**routine **co**simulation **t**est**b**ench
  - Start & stop simulation according to signal conditions
  - Full access to DUT hierarchy
  - More info @ public CERN seminar by Ben Rosser
- Python-based verification benefits from **extensive ecosystem & quick learning curve**
  - Complex tests & manageable “feature creep”
  - Automated, self-contained performance monitors
  - Contributions driven by non-experts & students



Flavors of simulation



Dense P&R logic of HCC

- Simulations run at
  - Register Transfer Level (hardware description language)
  - Post-synthesis (compiled to logic gates)
  - Place & Route (logic mapped to physical locations)
- ASICs tested standalone & all-together, connecting designs to form a **module = 1 AMAC, 2 HCCs, & 22 ABCs**
  - Corrected mismatches in complex inter-ASIC communication & configuration
- Test suite ran daily via continuous integration
  - 100's of unit tests give ~full coverage

Coverage report for HCC unit tests

Overall Instance-Based Coverage

Overall Average	Overall Covered	Block Average	Block Covered	Expression Average	Expression Covered	Toggle Average	Toggle Covered
96.54%	96.08% (58216/60590/5041)	99.54%	97.19% (6049/6224/310)	94.11%	93.19% (1150/1234/52)	94.50%	96.02% (51017/53132/4679)

Advanced module simulations

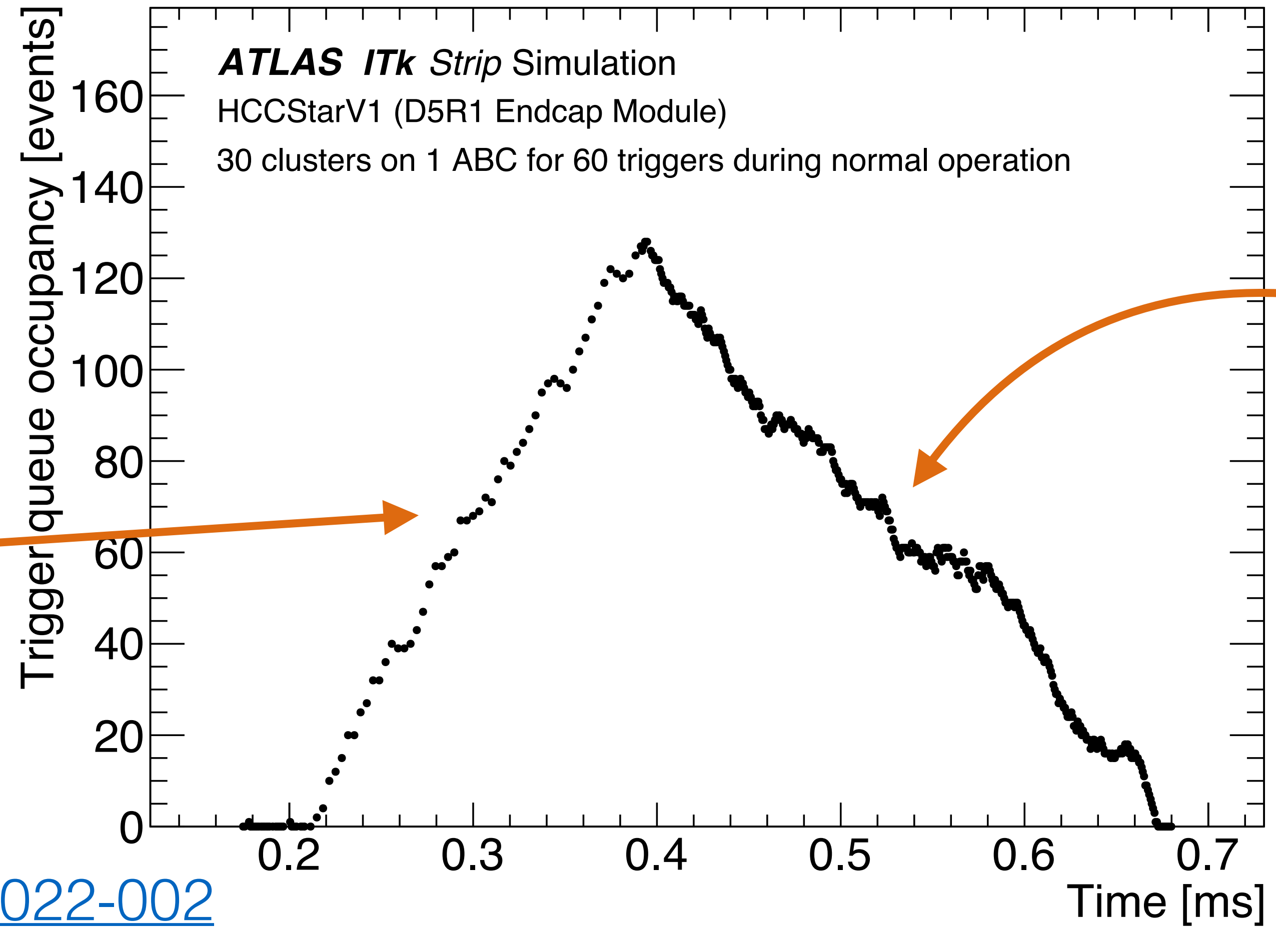
- Dozens of realistic tests w/ randomized data flow **based on HL-LHC expectations**
  - Trigger rates (~1 MHz), cluster occupancy (10-20 hits), signal timing (<25 ns), LHC beam structure
  - Long weekend tests for statistics + long-term behavior (1 hour real time = 7 ms simulation time)
- Scanned maximum operating rates, **easily exceed design requirements of 1 MHz triggering** for ~19 clusters per event (busiest expected @ HL-LHC)

Advanced module simulations

- Dozens of realistic tests w/ randomized data flow **based on HL-LHC expectations**
  - Trigger rates (~1 MHz), cluster occupancy (10-20 hits), signal timing (<25 ns), LHC beam structure
  - Long weekend tests for statistics + long-term behavior (1 hour real time = 7 ms simulation time)
- Scanned maximum operating rates, **easily exceed design requirements of 1 MHz triggering** for ~19 clusters per event (busiest expected @ HL-LHC)
- Studies of **anomalous noise bursts** show large operating margins, always with full recovery
  - Insights led to improvements to reset behavior for easier detector operation if / when necessary

Internal trigger queue occupancy rises during an extended cluster noise burst

ABCs are bottleneck during noise burst



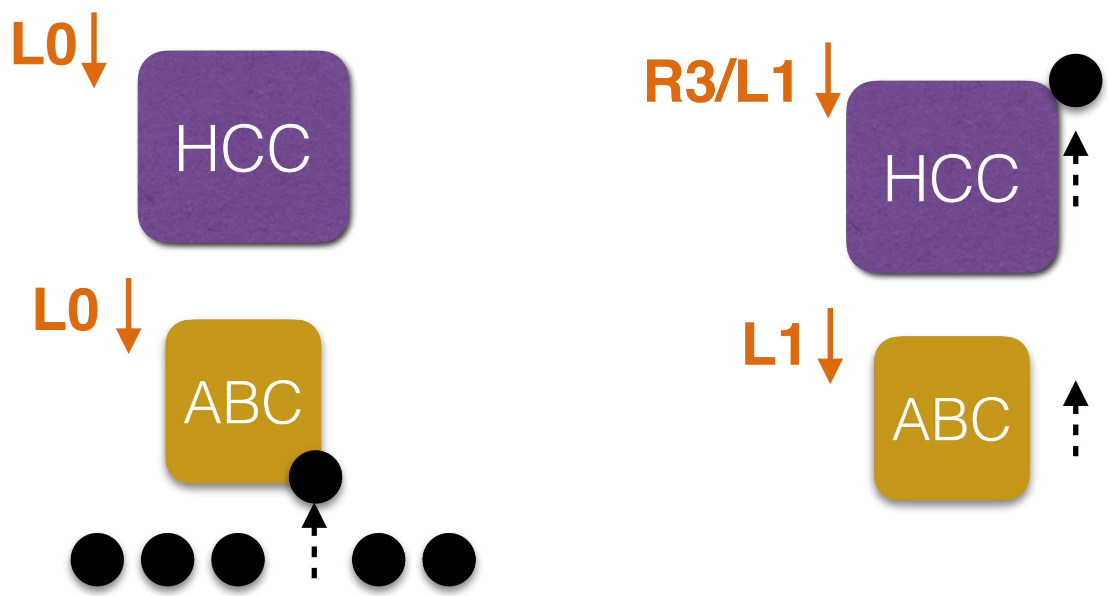
HCC catches up after burst ends

ITK-2022-002

Multi-level triggering

- Scrutiny of realistic performance metrics (trigger response latency, % data loss, etc.)
- Allowed feasibility studies of multi-level triggering
  - 3 trigger prioritization levels allow for on-detector track triggering

L0	R3	L1
preliminary trigger	**quick, intermediate**	**full detector readout**
ABCs store physics data (temporary)	~10% of detector ~5 μs latency	Needs decision before L0 overwrite



(Data every 25 ns)

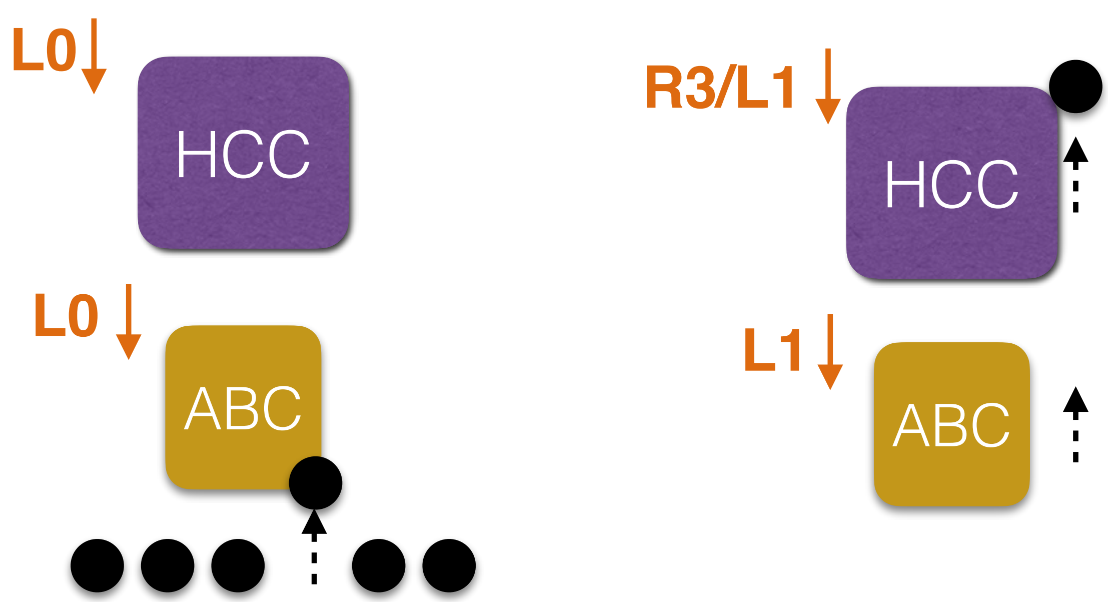
Multi-level triggering

- Scrutiny of realistic performance metrics (trigger response latency, % data loss, etc.)
- Allowed feasibility studies of multi-level triggering
  - 3 trigger prioritization levels allow for on-detector track triggering
- Realistic HL-LHC simulation informed operational phase-space of multi-level triggering
  - Not adopted for HL-LHC start, functionality remains for possible future adoption

L0
preliminary trigger
ABCs store physics data (temporary)

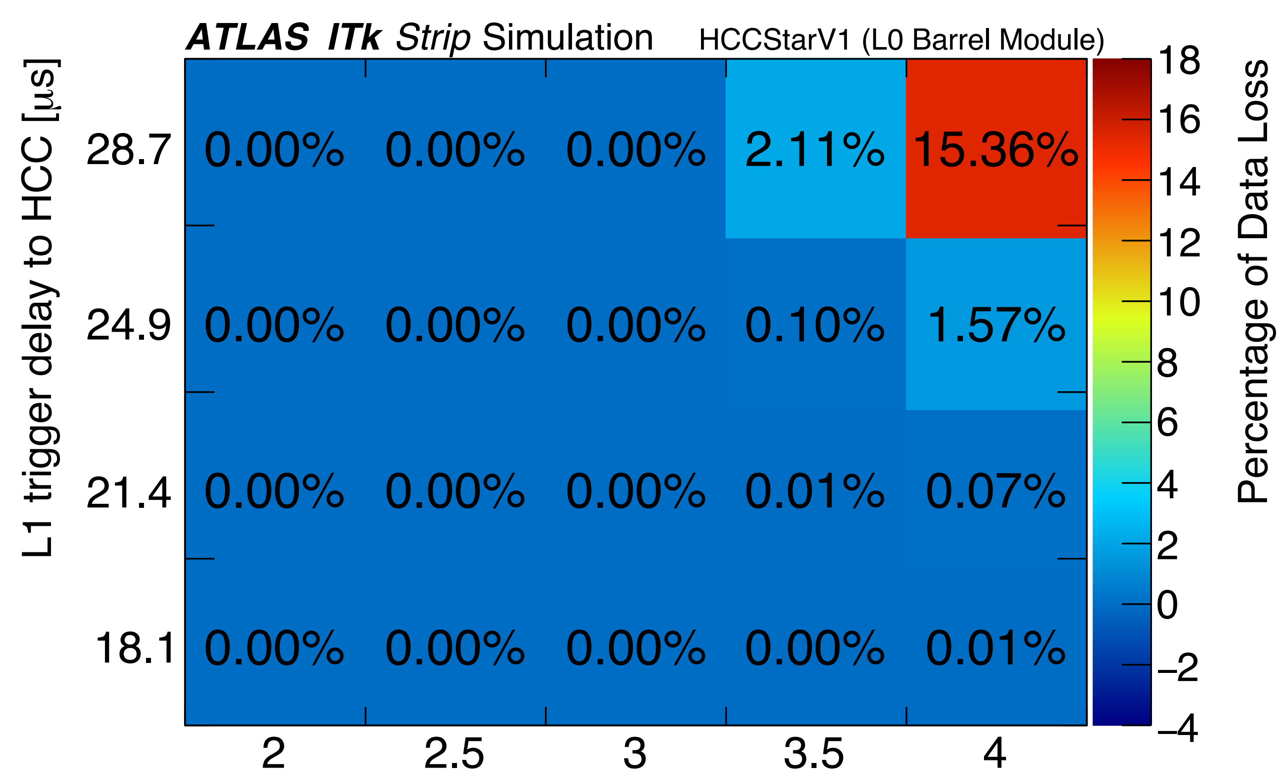
R3
quick, intermediate
~10% of detector
~5 μs latency

L1
full detector readout
Needs decision before L0 overwrite



(Data every 25 ns)

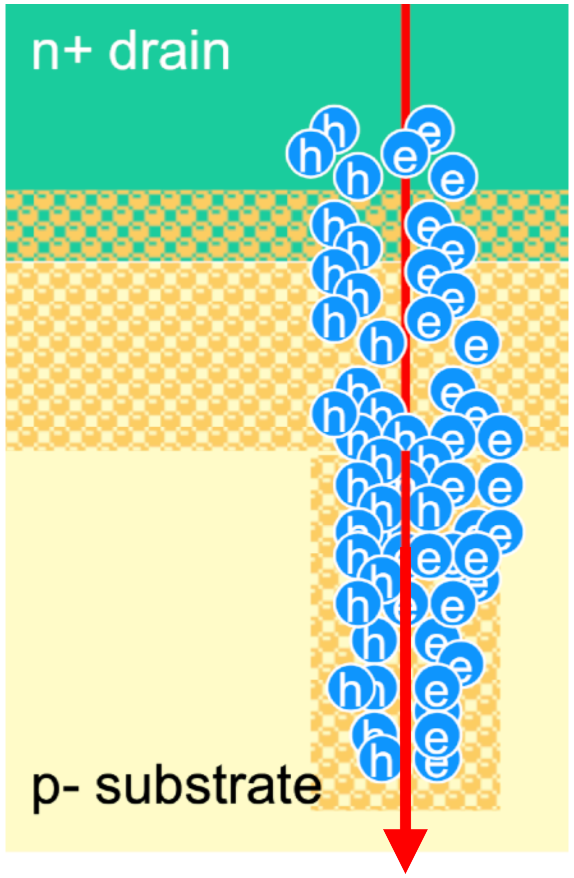
Data loss of multi-level trigger
(L0 rate vs L1 delay)



ITK-2022-002

Radiation concerns & protections

Sandro Bonacini

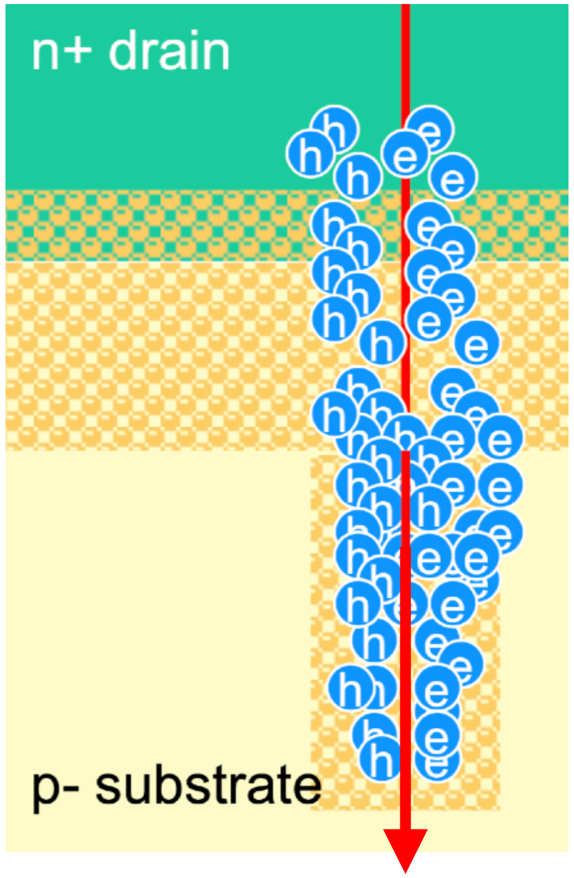


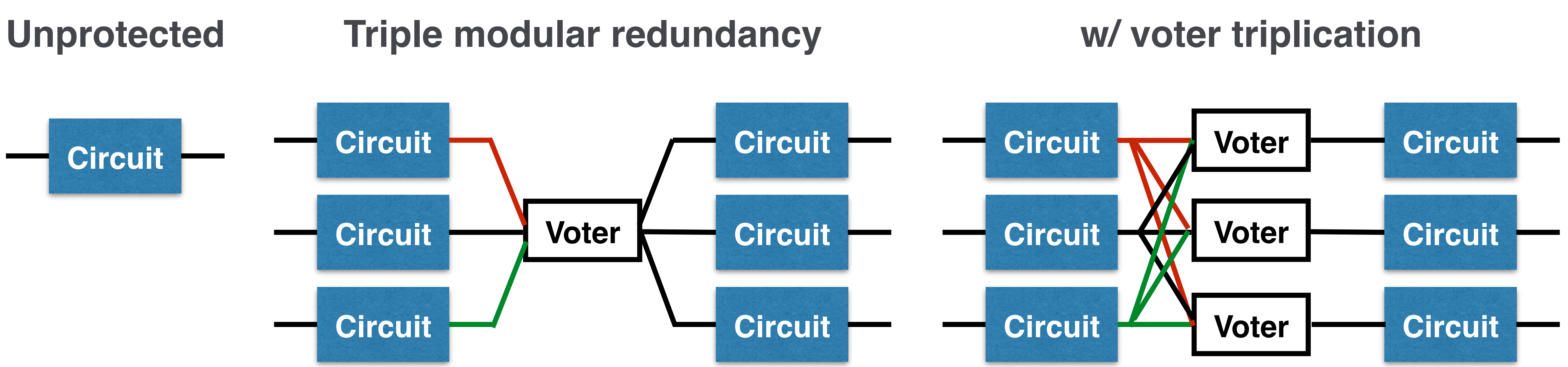
- ASICs subject to Single-Event Effects (SEE) from high energy particles
  - Single-Event Upsets (**SEU**): Ionizing particle causes **permanent state change** in flip-flop (`reg`)
  - Single-Event Transients (**SET**): Voltage pulse **temporarily inverts** logic gates (`wire`)
- "StarV0" design included initial protection:
  - Encoded inputs / outputs (6b8b / 8b10b), hamming encoding of finite-state logic
  - Some triplication of critical flip-flops, duplication of critical configuration registers

Radiation concerns & protections

- ASICs subject to Single-Event Effects (SEE) from high energy particles
  - Single-Event Upsets (**SEU**): Ionizing particle causes **permanent state change** in flip-flop (`reg`)
  - Single-Event Transients (**SET**): Voltage pulse **temporarily inverts** logic gates (`wire`)
- “StarV0” design included initial protection:
  - Encoded inputs / outputs (6b8b / 8b10b), hamming encoding of finite-state logic
  - Some triplication of critical flip-flops, duplication of critical configuration registers
- After demonstrated SEE sensitivities, “StarV1” focused on full protection:
  - **Deglitch circuits** on inputs / outputs
  - **Triple modular redundancy w/ voter triplication** (via CERN tmrg tool)

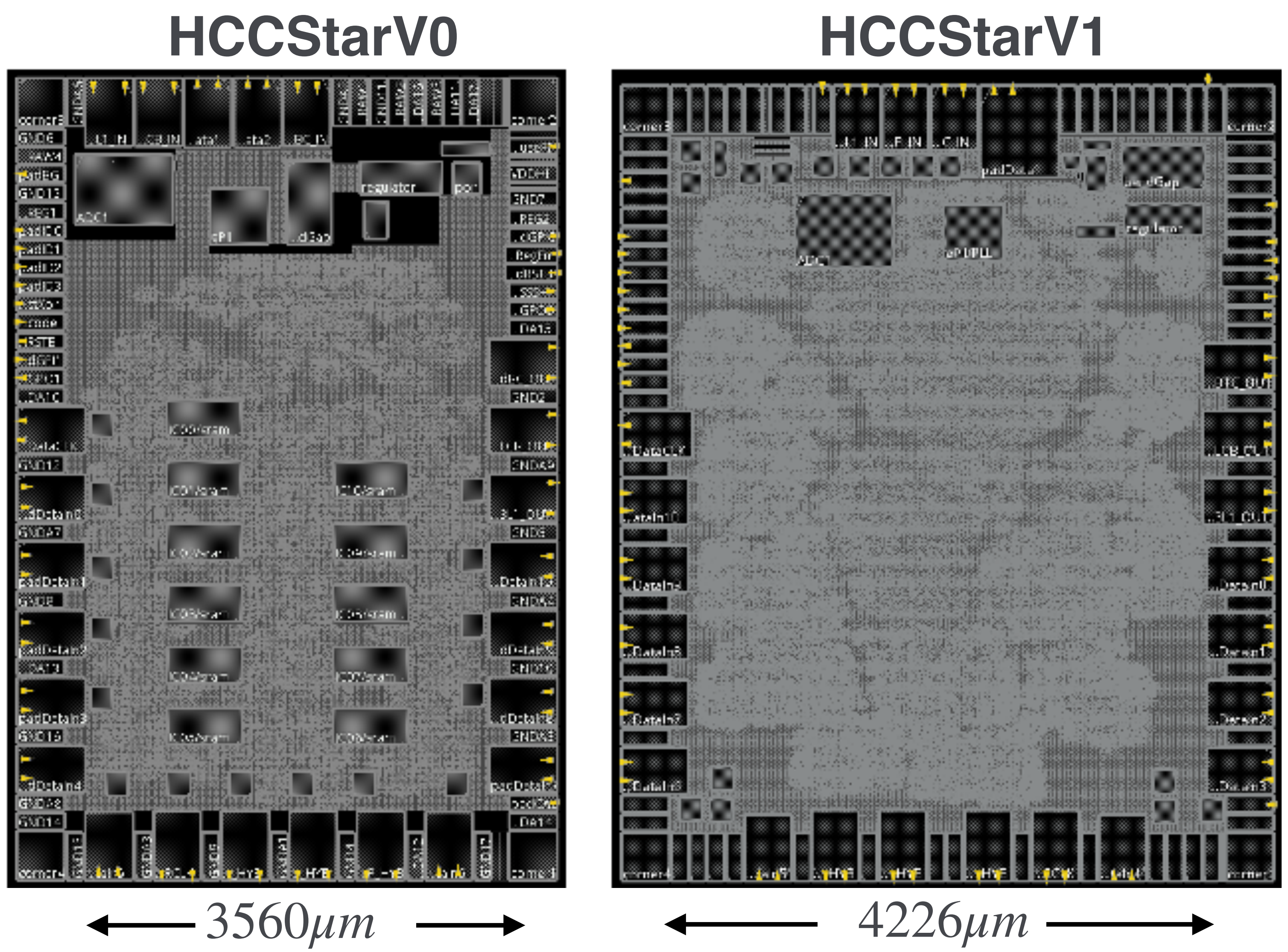
Sandro Bonacini





Tradeoffs of triplication

- Triplication is physically expensive & required design tradeoffs
  - Enlarged design footprint (HCC) & reworked floorplan to route congestion (HCC, ABC, AMAC)
  - Smaller memory buffers (HCC, ABC), replaced SRAM → FIFO (HCC)
  - Reduced set of observables automatically monitored (AMAC)
- Not triplicated: I/O & storage (physics data)



Radiation tolerance simulations for HCC

- Performed on all 3 ASICs, following will focus on HCC in module-level simulations
- SEE simulations inject logic flips during realistic data flow
  - Inject randomly using net list of all reg (SEU) & wire (SET) in the designs
  - Inject at 40+ MHz, as fast as possible while avoiding explicit double-SEEs
    - **~1 billion times faster than expected at HL-LHC**
  - SETs applied for 1 ns, longer than physically expected & correctable by deglitchers
    - 5 ns width also checked, total error rates agree within factor of 2
- Statistics target of **~100 SEEs** per reg (~42k) & wire (~250k) quickly exceeded via daily CI runs

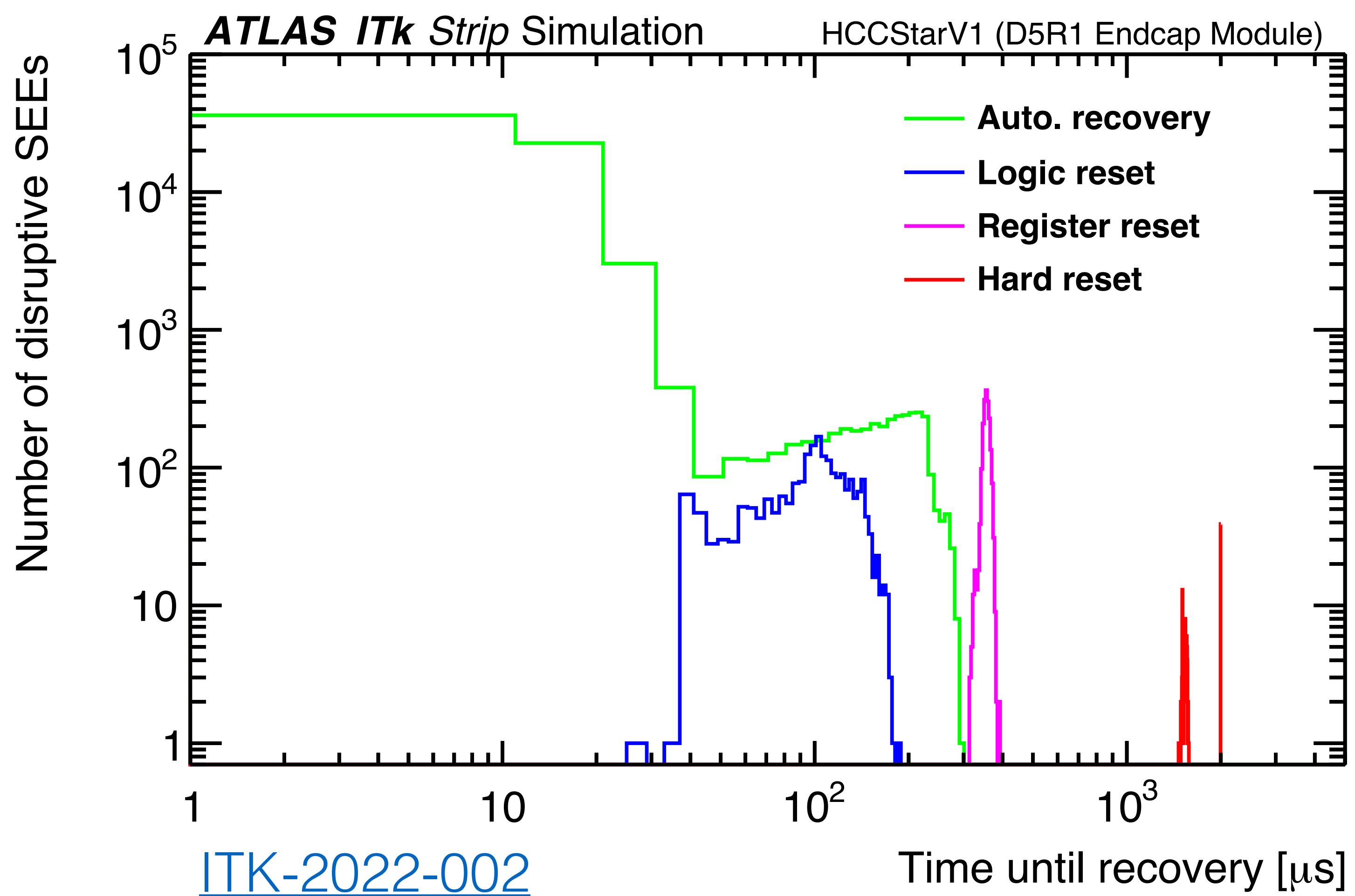
Radiation tolerance simulations for HCC

- Performed on all 3 ASICs, following will focus on HCC in module-level simulations
- SEE simulations inject logic flips during realistic data flow
  - Inject randomly using net list of all reg (SEU) & wire (SET) in the designs
  - Inject at 40+ MHz, as fast as possible while avoiding explicit double-SEEs
    - **~1 billion times faster than expected at HL-LHC**
  - SETs applied for 1 ns, longer than physically expected & correctable by deglitchers
    - 5 ns width also checked, total error rates agree within factor of 2
- Statistics target of **~100 SEEs** per reg (~42k) & wire (~250k) quickly exceeded via daily CI runs

- If data error observed, stop SEE injection & attempt escalating series of recoveries
  - **Automatic recovery**: No further errors within next 10 triggers
    - Commonly caused by **temporary corruption** of data itself (non-triplicated)
  - **Logic, Register, & Hard resets** set increasing amount of logic to power-on state

Example analysis of errors

- Automatically detect triplication errors by directly checking recovery of affected logic
  - Caught logic not refreshed after SEE, would have allowed SEEs to accumulate over time
- At high SEE rate difficult to associate error with single SEE (10+ μs delay)
  - **Statistical analysis** performed of nearby SEEs for all errors
  - Caught issues such as missing deglitchers on critical reset lines
- Result: enhanced radiation protections & insight into realistic operation + reset program



Time to recover
for each disruptive SEE

ITK-2022-002

Comprehensive SEE results

- **Triplicated logic** (92 million SEEs simulated): only 28 instances of *one-off* physics data corruption
  - “double SEEs” - individual SEEs propagate for short time before triplication corrects
  - Not expected @ HL-LHC (much slower SEE rate than simulation)

Comprehensive SEE results

- **Triplicated logic** (92 million SEEs simulated): only 28 instances of *one-off* physics data corruption
  - “double SEEs” - individual SEEs propagate for short time before triplication corrects
  - Not expected @ HL-LHC (much slower SEE rate than simulation)
- **Non-triplicated logic** (25 million SEEs simulated):
  - 0.3% caused *one-off* physics data corruption = $\mathcal{O}(1)$ error a day per HCC at HL-LHC
    - **10 orders-of-magnitude below electronic noise**
  - Resets performed for 0.01% of SEEs = $\mathcal{O}(1)$ error every 2 weeks per HCC at HL-LHC
    - Conservative upper bound, e.g. caused by accumulation of uncorrected SEEs (rare @ HL-LHC rates)
    - Errors are obvious, quick to identify & reset
  - All sources of hard resets were identified and corrected → **no hard resets necessary**

Comprehensive SEE results

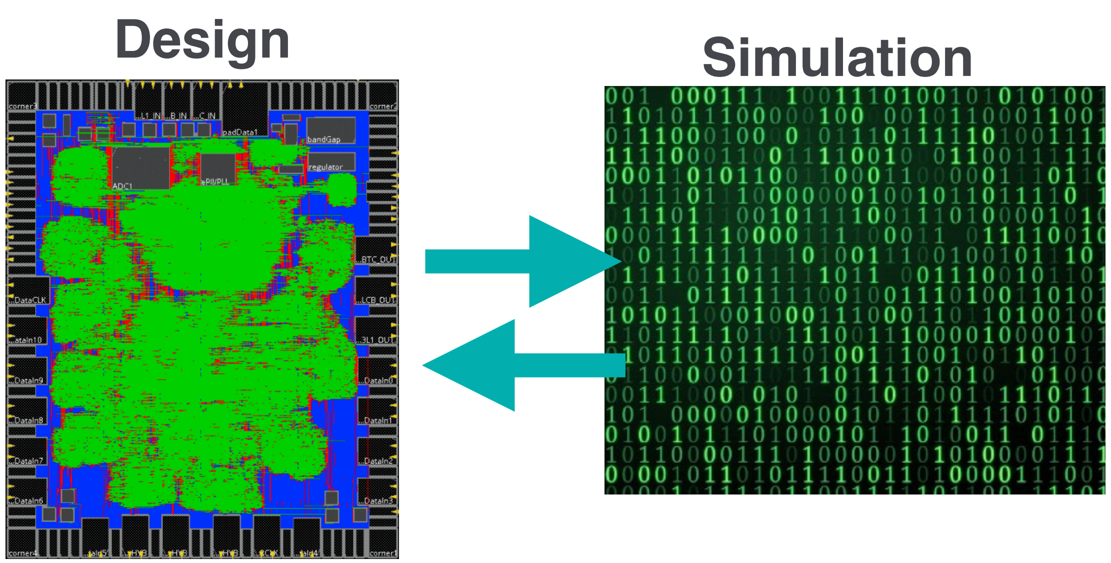
- **Triplicated logic** (92 million SEEs simulated): only 28 instances of *one-off* physics data corruption
  - “double SEEs” - individual SEEs propagate for short time before triplication corrects
  - Not expected @ HL-LHC (much slower SEE rate than simulation)
- **Non-triplicated logic** (25 million SEEs simulated):
  - 0.3% caused *one-off* physics data corruption = $\mathcal{O}(1)$ error a day per HCC at HL-LHC
    - **10 orders-of-magnitude below electronic noise**
  - Resets performed for 0.01% of SEEs = $\mathcal{O}(1)$ error every 2 weeks per HCC at HL-LHC
    - Conservative upper bound, e.g. caused by accumulation of uncorrected SEEs (rare @ HL-LHC rates)
    - Errors are obvious, quick to identify & reset
  - All sources of hard resets were identified and corrected → **no hard resets necessary**
- Results recently confirmed at TRIUMF & Louvain testbeams, see dedicated talks
  - Collaboration of engineers & physicists critical for identifying real deficiencies & red herrings

Irradiation Testing
Andie Wall, Wed @ 14:20

Functionality & Radiation Tolerance
Luis Gutierrez Zagazeta, Thur @ 16:40

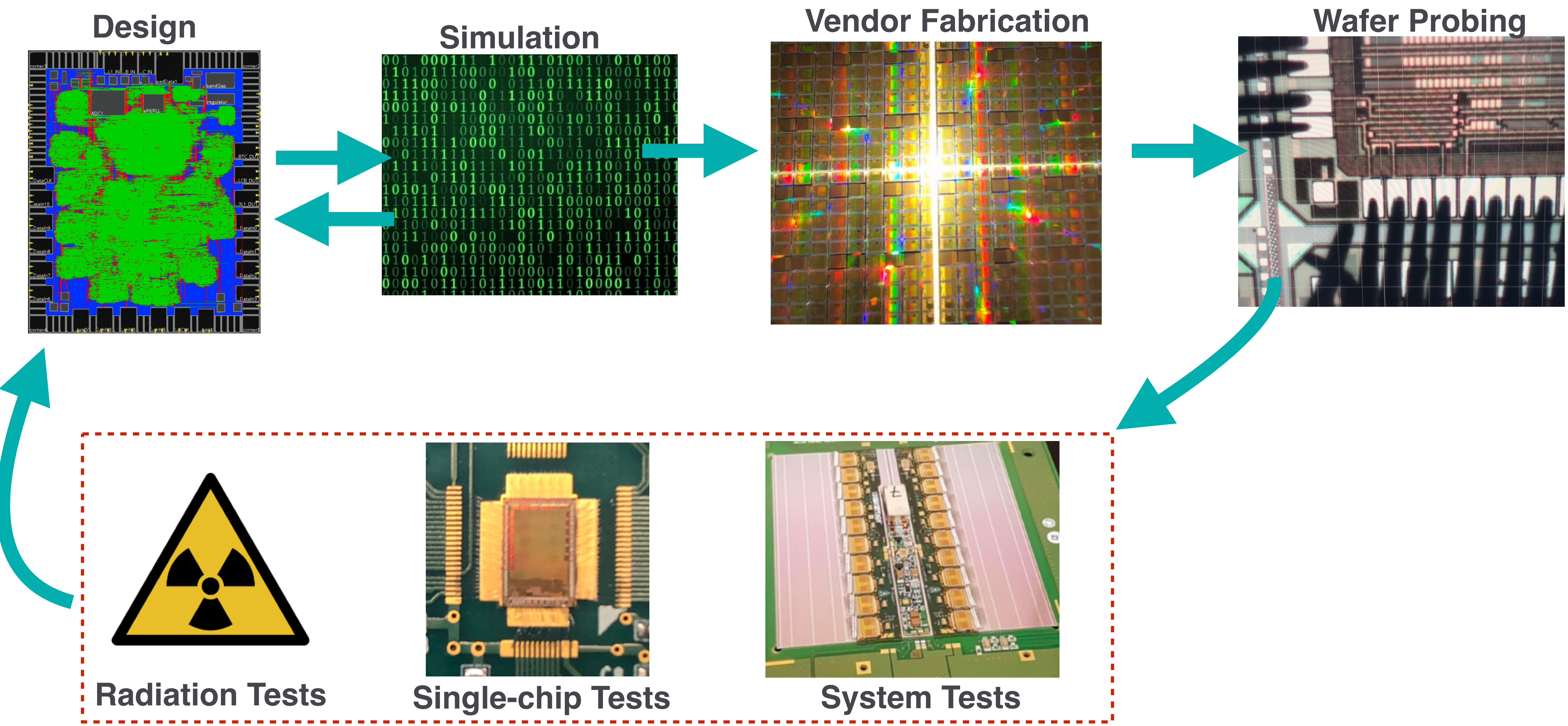
Conclusion

- Simulation of 3 ASICs and module-level interactions, streamlined by cocotb adoption
- SEE mitigation essential, benefits from shared community tools & best-practices
  - Novel, sophisticated simulation of radiation effects strengthened hardness of final ASICs designs



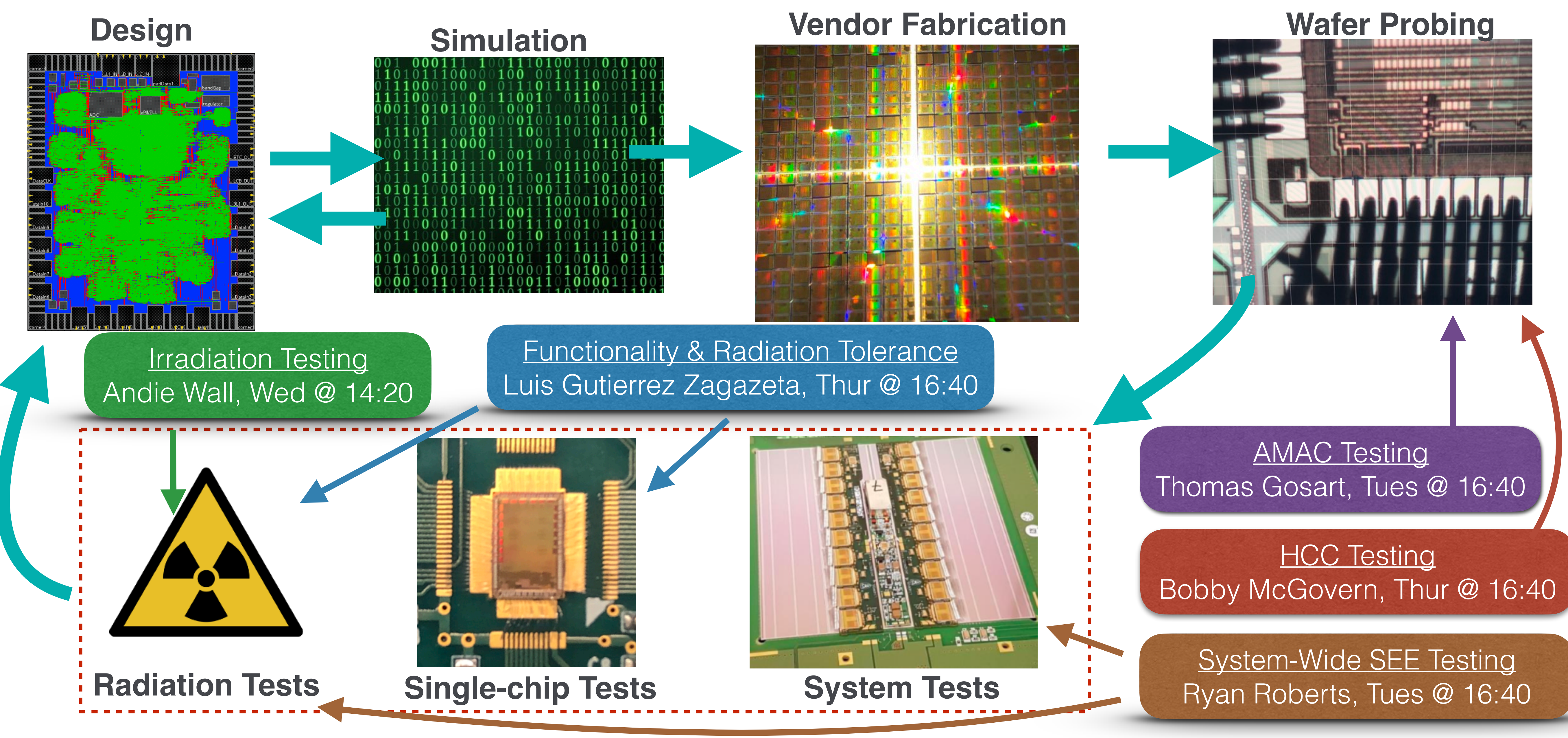
Conclusion

- Simulation of 3 ASICs and module-level interactions, streamlined by cocotb adoption
- SEE mitigation essential, benefits from shared community tools & best-practices
  - Novel, sophisticated simulation of radiation effects strengthened hardness of final ASICs designs
  - Experience gained w/ realistic operation informed successful functional, QA, & radiation testing



Conclusion

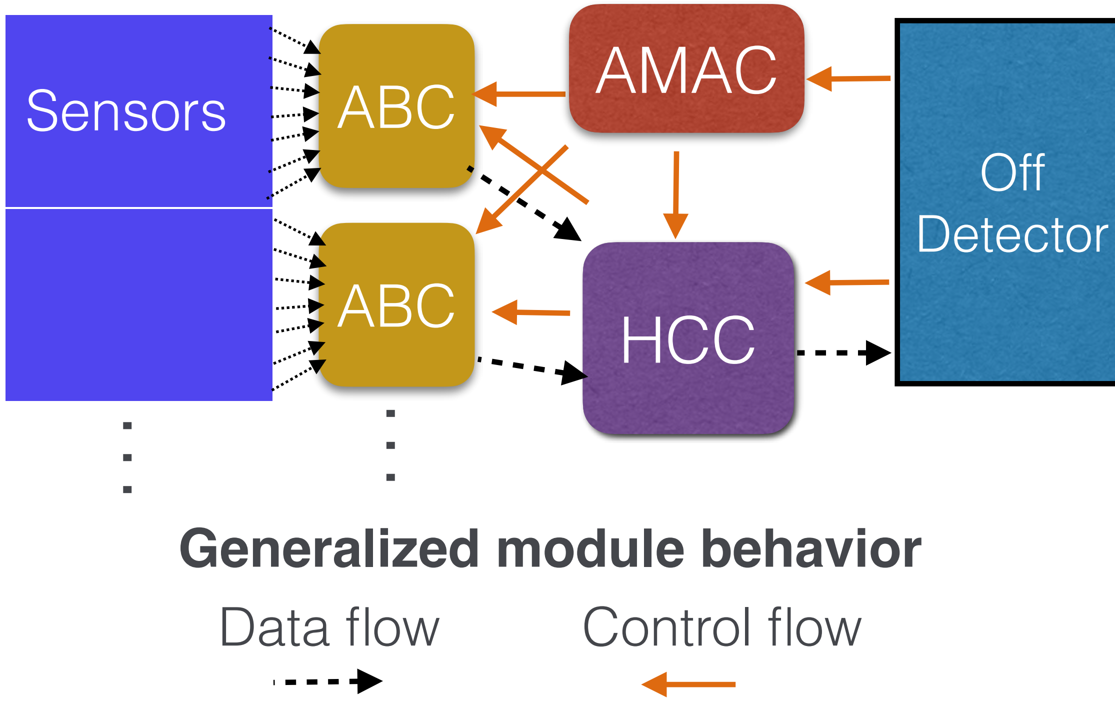
- Simulation of 3 ASICs and module-level interactions, streamlined by cocotb adoption
- SEE mitigation essential, benefits from shared community tools & best-practices
  - Novel, sophisticated simulation of radiation effects strengthened hardness of final ASICs designs
  - Experience gained w/ realistic operation informed successful functional, QA, & radiation testing



Backup

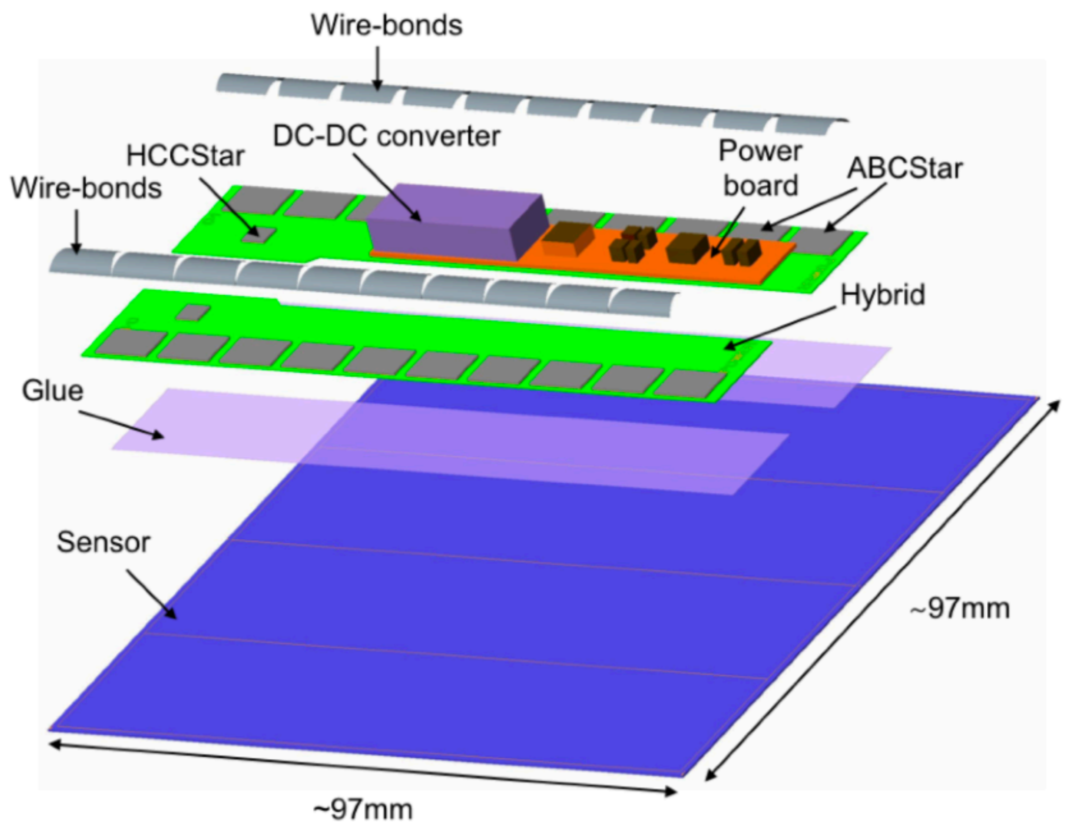
3 ASICs for ITk Strip detector

- Charged particles activate **strips of silicon sensors**
- **ABC** (ATLAS Binary Chip) reads 256 sensors, **digitize** & **compress data** into clusters
- **HCC** (Hybrid Controller Chip) **serializes data @ 640 MHz** for up to 11 ABCs, transmits commands & buffers trigger requests
- **AMAC** (Autonomous Monitoring And Control) - voltage / current / temperature **monitoring w/ automatic system interrupts**
- Several design iterations for evolving needs (bandwidth, rad-hard), **final** "**StarV1**" versions now approved

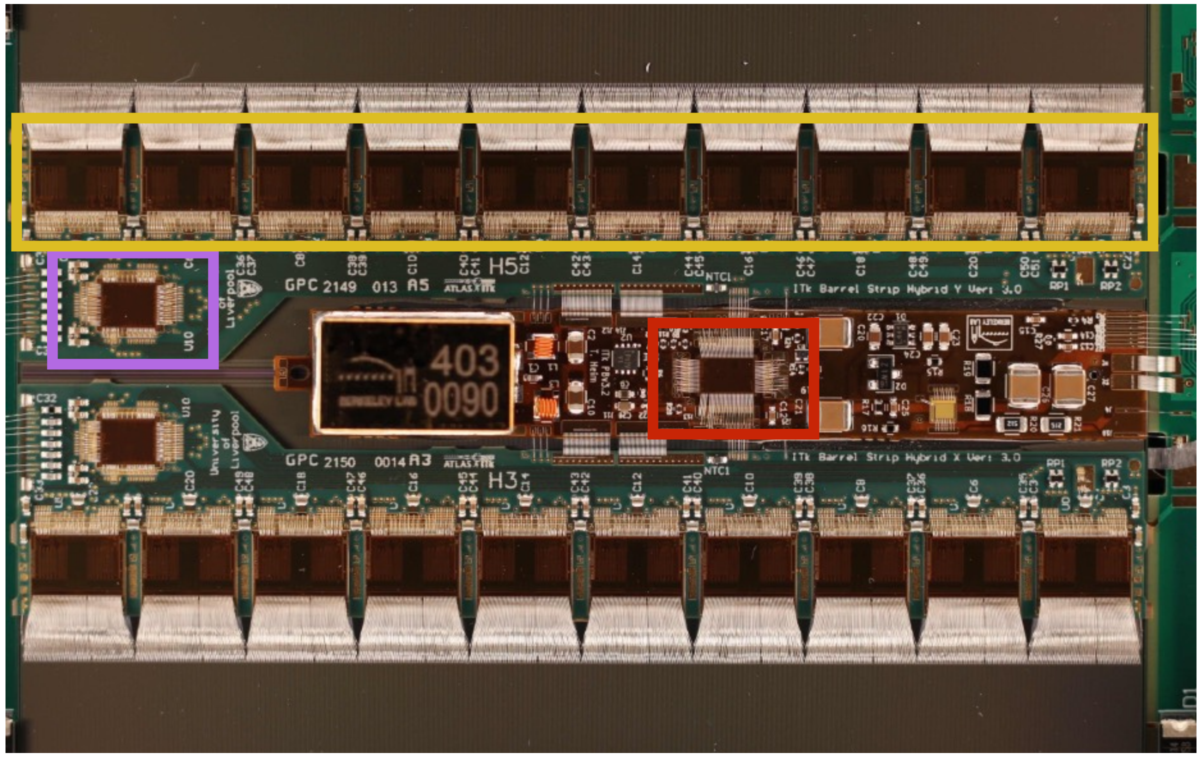


Generalized module behavior

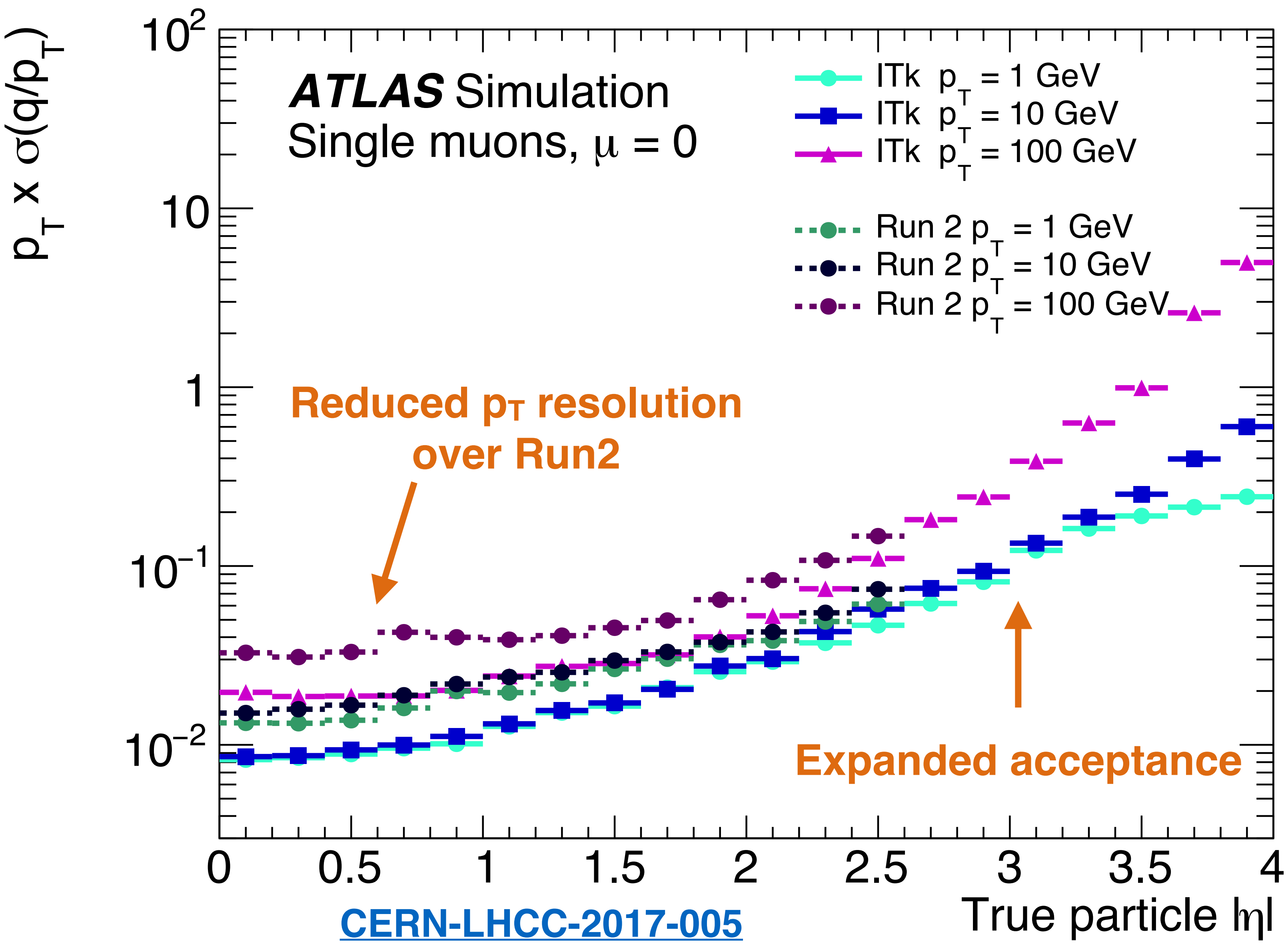
Exploded view of module components



Constructed module @ Brookhaven



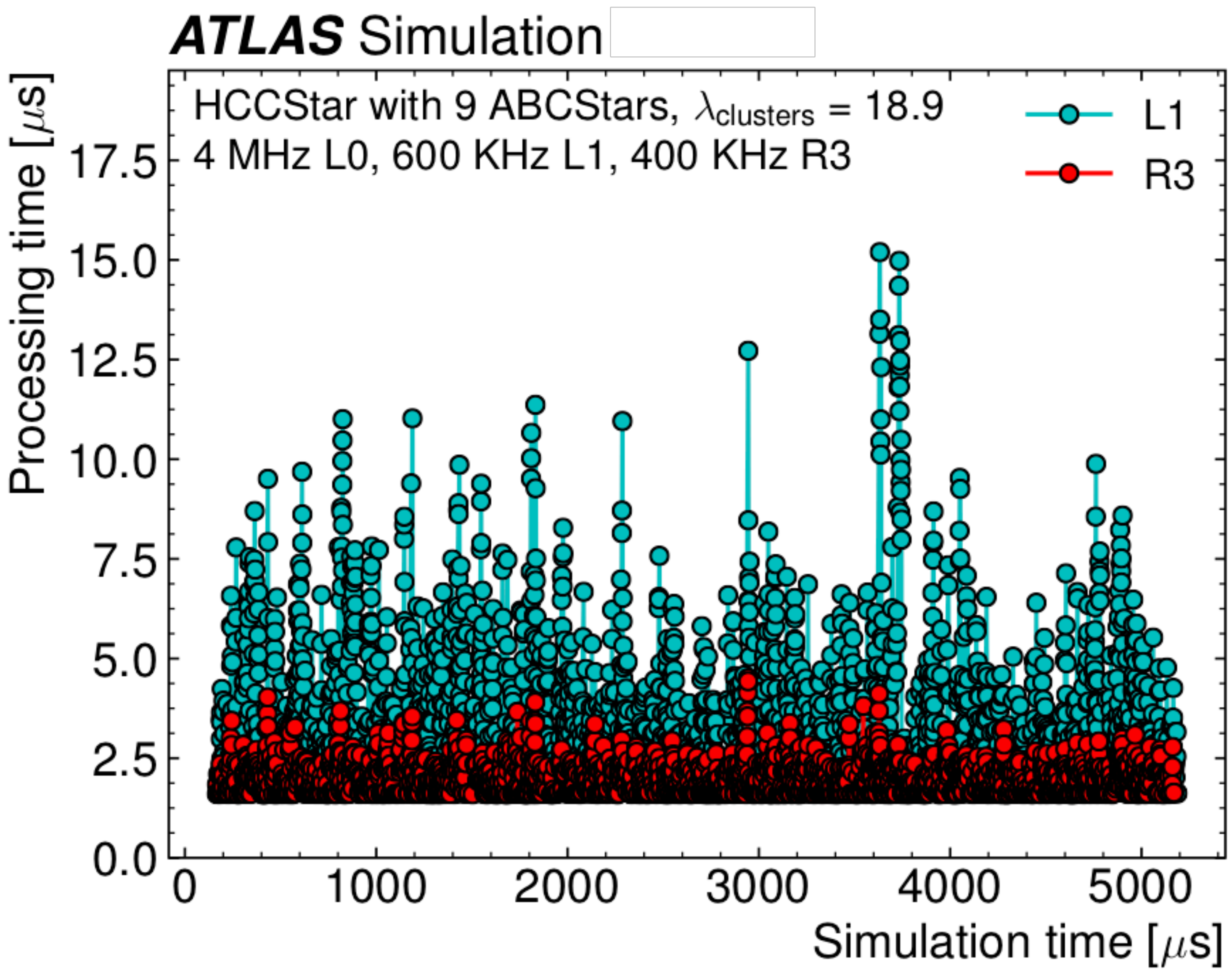
Tracking & physics improvements



CERN-LHCC-2017-005

Advanced simulations & measurements

Processing times for 2nd-level triggers
Low Priority (L1) & High Priority (R3)

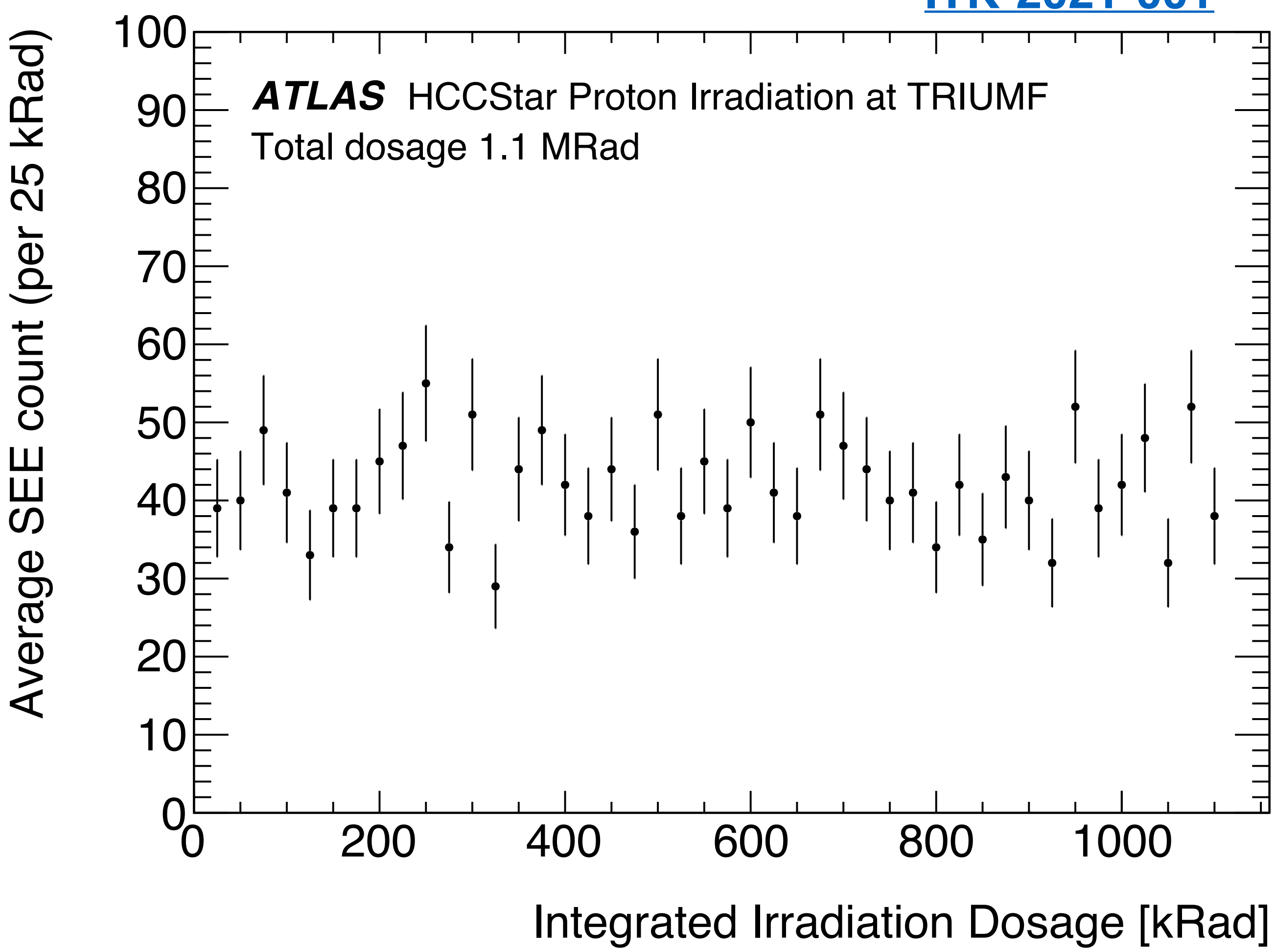


ITK-2021-001

Interpretation of SEE Results for HL-LHC

- Performed a rough, order-of-magnitude estimate of SEE rate at HL-LHC for non-triplicated logic
- Make a simplified extrapolation to **1000 SEEs per day for each HCCStar** at the HL-LHC, assuming:
  - Observed SEU rate of **40 SEUs per 25 kRad** in triplicated registers & logic from TRIUMF HCCStar V0 proton irradiations (figure below)
  - Rate of radiation exposure of **25 kRad per day** at the HL-LHC
  - **25x scale factor to non-triplicated logic** from rough comparison of register & wire counts in simulation
    - Assume equal probability of SEUs and SETs
- Simulated SEE rate is predicted to be **~1 billion times faster** than at HL-LHC

ITK-2021-001



Measured SEE rate in triplicated registers & logic during HCCStar v0 Proton Testbeam (18 registers, HPR logic, R3L1/LCB decoders)