Contribution ID: **57** Type: **Oral**

Simulated verification of the ASIC functionality and radiation tolerance for the HL-LHC ATLAS ITk Strip Detector

Tuesday, 20 September 2022 11:20 (20 minutes)

ASICs are important components in many HEP detectors and their functional simulation ensures successful operation while minimizing the number of long production cycles. Three radiation-tolerant ASICs (HCC, AMAC, and ABC) will perform the front-end readout, monitoring, and control of the outer layers of the ITk Strip particle tracker for the HL-LHC ATLAS detector. Simulated verification with the python-based cocotb framework allows for sophisticated tests with major contributions from students and firmware non-experts. The verification program includes interactions between multiple ASICs, realistic HL-LHC data flows, operational stress tests, and a focus on mitigation of disruptive Single Event Effects due to radiation.

Summary (500 words)

ASICs are an important component of many particle detectors and are often required in quantities of 100,000 or more. ATLAS is one such detector and will replace the charged particle tracker with a new Inner Tracker (ITk) for the HL-LHC upgrade. The ITk is designed for a faster data readout, finer granularity, and ability to operate in a high radiation environment of up to 1.7 GigaRad. To achieve this three custom ASICs were designed for the outer ITk Strip subdetector. The ATLAS Binary Chip (ABC), Hybrid Controller Chip (HCC), and Autonomous Monitoring and Control (AMAC) chip each have an essential role in data readout, control, and monitoring that will be discussed. Together these highly-integrated electronics control a complex detector readout system.

ASIC development is a shared bottleneck across the HEP community, with every ASIC version requiring significant time and cost for design, production, and testing. A comprehensive program of simulated functional verification is essential for minimizing the number of development cycles and ensuring a robust design. We' ve implemented simulations using the python-based cocotb framework interfaced with the Cadence Incisive simulator. This relatively new framework has allowed for sophisticated tests to be developed within a python ecosystem, with contributions driven by students and firmware non-experts. The cocotb framework has been sponsored by the FOSSi Foundation and is actively developed, and our experience with these open-source tools would be of interest to the community.

A test suite was developed to run automatically and regularly via Continuous Integration on the RTL, post-synthesis, and place-and-route designs. Unit tests explored specific functionality and maximized the design coverage. System tests simulated all three ASICs together and directly connected their inputs and outputs. Realistic data flows were injected that mirrored the expected HL-LHC proton beam structure, with realistic occupancies and signal timing. Specialized tests measured the maximum readout rates of the combined system, and stress tests injected specified bursts of data requests or noise. We measured latencies between and within ASICs and memory occupancies, providing detailed understandings of the multi-ASIC system.

To operate under high radiation conditions the ASICs have protections against disruptive Single Event Effects (SEEs) including Triple Modular Redundancy with triplicated voters of logic, wire deglitchers, and encodings for various FSMs and signals. The simulations were run while randomly injecting SEEs that flipped logic states or as transients that temporarily inverted signals on wires. To ensure rare failures would be observed, SEEs were injected at a much faster rate than expected at the HL-LHC and simulations were run in parallel

daily for a large length of time. A careful review of waveforms also identified and corrected numerous SEE sensitivities, and statistical analysis correlated various observed errors with specific SEEs. The simulations gave detailed knowledge of how errors may appear, what specific actions were required given observations, and the timescales for recovery.
This novel simulation test suite brought a new degree of thoroughness and realism to studies of a complex system with multiple ASICs, giving confidence to the design.

Primary authors: NIKOLICA, Adrian (University of Pennsylvania); DANDOY, Jeff (University of Pennsylvania (US)); WALL, Andie (University of Pennsylvania (US)); ROSSER, Benjamin John (University of Chicago (US)); MCGOVERN, Bobby (University of Pennsylvania (US)); THOMSON, Evelyn Jean (University of Pennsylvania (US)); MAYERS, Godwin (University of Pennsylvania); KROLL, Joseph Ira (University of Pennsylvania (US)); GUTIERREZ ZAGAZETA, Luis Felipe (University of Pennsylvania (US)); REILLY, Michael Bendl (University of Pennsylvania (US)); NEWCOMER, Mitchell Franck (University of Pennsylvania (US)); DRESSNANDT, Nandor (University of Pennsylvania (US)); KEENER, Paul (University of Pennsylvania (US)); LU, Sicong (University of Pennsylvania (US)); GOSART, Thomas Christopher (University of Pennsylvania (US)); ASHMANSKAS, William (University of Pennsylvania (US))

Presenter: DANDOY, Jeff (University of Pennsylvania (US))

Session Classification: ASIC

Track Classification: ASIC