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Radiation-Tolerant All-Digital Clock Generators for HEP Applications

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The emergence of high-precision timing systems in High Energy Physics motivates new developments in the domain of clock generation and distribution. Particularly when considering the challenges arising from adopting advanced deep-submicron CMOS technology nodes, All-digital Phase Locked Loop (PLL) and Clock and Data Recovery (CDR) architectures constitute a promising option for future High Energy Physics (HEP) experiments. Both LC-oscillator as well as a ring oscillator based All-Digital front-end PLL/CDR blocks were studied, designed, manufactured and characterized. The design process, important radiation hardening considerations, as well as the performance obtained with these circuits will be presented in this talk.

Summary (500 words)

Timing detectors foreseen for the High-Luminosity LHC have pushed the performance requirements for clock signals in terms of their stability and random jitter to the level of picoseconds. Currently, such clock signals are typically generated using high-performance on-chip PLL circuits, implemented using conventional analog/mixed-signal architectures. The adoption of more advanced deep-sub-micron CMOS nodes for HEP ASICs reduces the voltage headroom and signal-to-noise ratio available in such precision analog circuits, making their implementation increasingly difficult. All-digital clock generator architectures, having found widespread adoption in commercial applications, systematically mitigate many scaling-related challenges and enable generation of high purity clock signals even in the most advanced CMOS technology nodes to date. Conceptually, the All-Digital PLL (ADPLL) approach replaces most of the critical analog circuits found in conventional architectures (charge pumps, analog filters, etc.) by their equivalents in the digital domain.

With respect to the radiation environments found in particle accelerator environments, the adoption of digital architectures for clock generation circuits can offer multiple benefits: Digital circuits allow reliable single-event effects (SEE) mitigation. Since the dependence on MOS transistor device parameters sensitive to radiation is reduced in digital circuits, their total ionizing dose (TID) response can be significantly improved.

With these considerations in mind, two all-digital clock generator circuits compatible with typical front-end system requirements have been studied and implemented. The developed macro blocks allow operation in both phase-locked loop (PLL) and clock and data recovery (CDR) modes of operation, supporting reference clock frequencies of 40 - 320 MHz as well as input data rates of 40 - 320 Mbps. Three programmable clock outputs provide any combination of 40, 80, 160, 320, 640 or 1280 MHz signals to downstream systems. To cater to the requirements of different types of systems, both a high performance (LC-oscillator based) as well as a general-purpose (ring oscillator based) flavor of this block were designed and characterized and their individual trade-offs studied extensively. Single-event effects tolerance of the digital circuit blocks comprising the proposed ADPLL/CDR design is achieved by triple modular redundancy (TMR). The different digitally controlled oscillator (DCO) architectures have been individually studied and hardened against both TID and SEEs using circuit-level radiation hardening by design (RHBD) techniques.

Both circuits manufactured in a 65nm CMOS technology are shown to be compatible with the requirements of contemporary HEP systems and were shown to exhibit excellent radiation tolerance: SEE tolerance was studied using heavy ion irradiation up to 63 MeV.cm^2/mg, and both types of ADPLL were shown to operate correctly up to a total dose of 1.5 Grad(Si). To study the performance of these circuits within commonly used system architectures, the developed test chip has been incorporated into a Versatile Link+ (VL+) test system,

comprised of an FPGA back-end, an optical high-speed link and an lpGBT ASIC. Operation of both all-digital clock generator circuits with excellent jitter performance (<5 ps rms) as well as low power dissipation (11 mW @ 1.2 V) and full compatibility with typical systems requirements is demonstrated in this configuration.

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