Contribution ID: **100** Type: **Oral**

A 64 channels ASIC for the readout of the silicon strip detectors of the PANDA Micro-Vertex Detector

Tuesday, 20 September 2022 12:00 (20 minutes)

The ToASt ASIC is a 64 channel integrated circuit designed for the readout of the Silicon Strips that will equip the Micro-Vertex Detector of the PANDA experiment.
The ASIC is synchronous to a 160 MHz clock, which defines also the time resolution. A common time stamp is distributed to all channels to provide a common time reference for time of arrival and time over threshold measurements. Two 160 Mb/s serial lines provide the interface to the data concentrator.
ToASt is implemented in a commercial 110 nm CMOS technology with triplicated logic to protect against single event upsets.

Summary (500 words)

The Micro Vertex Detector (MVD) of the PANDA experiment will consists of two parts, a barrel section around the interaction point and a disk section in the forward position. The two sections will be equipped with both Silicon Pixel and Strip Detectors (SPDs and SSDs).
The ToASt ASIC is a 64 channel integrated circuit designed for the readout of the PANDA SSDs. Its analog front-end is divided in two parts. The first one is made of a charge sensitive preamplifier which can be programmed to accept signals of both polarities, a programmable shaper and a current buffer. The second part consists of a Time-over-Threshold (ToT) stage with linear discharge and two comparators with independent thresholds. The double threshold information can be used to reduce the time jitter on small signals by sampling the time information with a low threshold, where the signal edge is faster, while using a higher threshold to validate the event, thus reducing noise events.
The arrival time of the two edges of the comparator is measured by storing the corresponding value of a global time stamp reference, which is distributed to all channels. The time of arrival and ToT informations are therefore provided by the rising edge time stamp and the difference between the two time stamps, respectively.
The channels are grouped in regions made of 8 channels each, which provide local buffering. The event information is packed in a 32 bit word and transmitted over two serial links at 160 Mb/s by a global controller.
The ASIC is designed in a commercial 110 nm CMOS technology. The die size is 4.4 mm x 3.2 mm. In order to simplify the board design when multiple ToASts are used to read-out a large SSD, the I/O pins are all located either at the top or at the bottom of the die. The digital logic has been triplicated in order to protect against Single-Event Upsets (SEUs).
The ToASt ASIC has been succesfully tested in laboratory. The non-linearity

of the ToT gain is below 0.64% (r.m.s.) in the range 1.5-16 fC, while for higher input signals (up to 66 fC) a gain compression is observed.
The ToT gain spread among channel is fairly large but can be reduced to less than 2% for gain ranges between 55 and 65 ns/fC via integrated channel calibration DACs.
The time jitter is below one clock cycle (6.25 ns) for the leading edge and around 3 clock cycles for the trailing edge. The amplitude noise is around 300 e- with no detector connected. The power consumption is 180 mW.
Further tests are foreseen in the next months, including the test of the ASIC connected with a detector and irradiation tests.

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Session Classification: ASIC

Track Classification: ASIC