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TimeSPOT ASIC developments for 4D-Tracking

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We present the timing measurements performed using the Timespot1 ASIC after hybridization onto a sensor pixel matrix featuring 32x32 channels. The ASIC is fabricated in CMOS 28-nm technology and integrates 1024 readout pixels, each equipped with a fast Analog Front End and a high-resolution TDC. The sensor is a matched matrix of 1024 3D silicon sensors, having pitch of 55 µm and processed in a so-called trench geometry, highly optimized for timing. Such sensor technology has been already proven to be capable of an intrinsic timing resolution around 10-ps per hit.

Summary (500 words)

Pixels with timing capabilities (also known as 4D pixels) are of crucial importance for the inner trackers of the next generation of collider experiments. The given requirements for such detectors are very challenging: timing resolution per hit of at least 50 ps and concurrent space resolution in the range of 10 µm and high rates. As an example, the LHCb-Upgrade-II VELO requires up to 350 kHz per pixel. Furthermore, high radiation resistance is necessary both for the sensors (around 5x 1016 1 MeV neutron equivalent per cm2) and the electronics (2 Grad). Concerning the readout ASIC, this task is particularly hard, as such performance should be reached within severe limits in power consumption and silicon area budget (typically 1.5 W/cm2 or less).
Sensors capable to reach the needed timing resolution have been already developed. 3D-trench silicon sensors reach an intrinsic time resolution of 10 ps [1] and clearly demonstrate that the readout electronics is the real bottleneck towards system performance.
The Timespot1 ASIC has been developed to attack the challenge and study in detail technological and design constraints. Timespot1 is designed in CMOS 28 nm technology. It features a 32×32-pixel matrix with a pitch of 55 µm. The ASIC is conceived to be capable of reading-out pixels with timing resolution below 50 ps on the full chain (sensor, amplifier, Time-to-Digital-Converter). Each pixel is endowed with a charge amplifier, a leading-edge discriminator with offset compensation, and a Time-to-Digital Converter with time resolution around 30 ps and maximum read-out rate of 3 MHz per pixel.
After successful test-bench characterization [2], the ASIC has been hybridized onto a matched 3D-trench sensor and tested in the laboratory using laser-beam pulses and in a test-beam setup against charged minimum ionizing particles. Each hybrid, housed on a dedicated PCB, represents an elementary tracking layer. Up to 8 layers can be readout together by a dedicated acquisition system, based on a Xilinx KC705 commercial board. This paper presents the results out of the hybrid tests and illustrates the main system criticalities emerged in terms of system design parameters. They represent clear indications along the path of such an important development in electronics.

[1] D. Brundu et al., Accurate modelling of 3D-trench silicon sensor with enhanced timing performance and comparison with test beam measurements, JINST 16 (2021) 09, P09028.
[2] L. Piccolo et al., First Measurements on the Timespot1 ASIC: a Fast-Timing, High-Rate Pixel-Matrix Front-End, arXiv:2201.13138 [physics.ins-det]. To be submitted to IEEE TNS.

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