## **TWEPP 2022 Topical Workshop on Electronics for Particle Physics**



Contribution ID: 110

Type: Oral

## Development of a Stitched Monolithic Pixel Sensor prototype (MOSS chip) towards the ITS3 upgrade of the ALICE Inner Tracking System

Wednesday 21 September 2022 09:00 (20 minutes)

The MOnolithic Stitched Sensor chip (MOSS) is a development prototype towards the innovative ITS3 vertexing detector for the ALICE experiment at the LHC. Designed using a 65 nm CMOS Imaging technology, it aims at profiting from the stitching technique to construct a single-die monolithic pixel detector of 1.4 cm x 26 cm. The MOSS chip is one of the prototypes developed within CERN-EP R&D to learn how to make stitched wafer-scale sensors with satisfactory yield. This contribution will describe the challenges encountered and some of the techniques adopted in the design of the chip.

## Summary (500 words)

The ALICE collaboration is pursuing the development of a novel and considerably improved vertexing detector called ITS3 to replace the three innermost layers of the Inner Tracker System during the Long Shutdown 3 of the LHC. The primary goals of the upgrade are to reduce the material budget, targeting the unprecedented value of 0.05% X0 per layer, and to place the first layer at a radial distance of 18 mm from the interaction point. The impact parameter resolution will improve by a factor two over all momenta and the tracking efficiency at low transverse momentum will drastically increase.

The new detector will consist of three cylindrical layers, with each half-cylinder constituted by monolithic sensors bent at radii of 18, 24 and 30 mm. The length of each wafer-scale silicon die in the beam direction is about 26 cm and the widths of the dies on the three layers are about 56, 75 and 94 mm. Significant material reduction is achieved with cooling by air flow and avoiding or minimising other external components, including flexible circuits, in the active area.

A first step towards this objective is the MOnolithic Stitched Sensor (MOSS) prototype. Developed using a commercial 65 nm CMOS Imaging technology, it aims at profiting from the stitching technique on 12"wafers to manufacture a single-die sensor of 1.4 cm x 26 cm. The primary goal of the MOSS prototype is to learn how to make a stitched monolithic particle detector with a satisfactory yield.

The MOSS prototype features one left endcap, 10 repeated sensor units and one right endcap. Every repeating sensor unit is subdivided into two halves, top and bottom, each with 4 pixel matrices. The pixel pitch in the top half is of 22.5 um and of 18.0 um in the bottom half. The two pixel pitch values are intended to compare the yield with different layout densities and spacing margins. Every top and bottom halves of the repeating sensor unit have an independent supply, both for analog and digital power, totalizing over 40 distinct supply nets for the matrices and peripheries on the whole chip. This powering granularity allows maintaining off single repeating sensor units in case of manufacturing defects potentially causing short circuits that could otherwise affect the entire chip.

Data transmission over the 26 cm of silicon is prototyped by means of a backbone bus crossing the stitching boundaries which features an independent power supply.

Each half repeating sensor unit can be isolated from the stitched backbone bus and independently operated through dedicated pads on the long edge of the chip.

A global serial port and a data transmission port are available in the left endcap edge to demonstrate and study readout and control of all the repeated units from a common interface at one edge of the chip.

This paper will discuss the challenges encountered and some of the techniques and solutions adopted at various levels in the design of the innovative MOSS prototype chip.

Primary author:VICENTE LEITAO, Pedro (CERN)Presenter:VICENTE LEITAO, Pedro (CERN)Session Classification:ASIC

Track Classification: ASIC