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From the first full chain precision timing prototype ETROC1 (4x4) to the first full size full functionality ETROC2 (16x16) for CMS MTD Endcap Timing Layer (ETL) upgrade

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The Endcap Timing ReadOut Chip (ETROC) is designed to process LGAD signals with time resolution down to about 40-50ps per hit. The ETROC1 has been extensively tested, another round of beam test is now on going at Fermilab since March 2022. The performance of ETROC1 will be summarized, with emphasis on the main issue learned on the 40MHz noise after bump bonded with LGAD sensor and most recent beam test results. The ETROC2 design will be presented, to be submitted in summer 2022, including the development strategy from ETROC1 to ETROC2 and how the 40MHz noise issue is addressed.

Summary (500 words)

The ETROC1 is the first full chain precision timing prototype, aiming to demonstrate the performance of the full signal processing chain, with the goal to achieve 40 to 50 ps time resolution per hit with LGAD (thus ~30 - 35ps per track with two detector layer hits). The bare ETROC1 chips have been tested extensively using charge injection, and the measured performance agrees well with the simulation, including the power consumptions. The bump bonded ETROC1 chips (with LGAD sensors) have encountered a noise originated from its own 40MHz readout clock and coupled via the bump bonded sensor into the preamplifier input. Because of that, the discriminator threshold has to be increased (from ~3fC to ~8fC) in order to minimize the noise impact during beam test. For the beam tests, because the LGAD can provide enough signal gain, this is not an issue and one can therefore study the timing performance with the increased discriminator threshold. The timing performance of the full signal processing chain of the 4x4 pixel array has been studied this way using a beam telescope with three layers of bump bonded ETROC1/sensors. Time resolution on the order of 42-45 ps per hit has been achieved during the beam tests in 2021 as well as 2022, and this is consistent with the expectation from simulation. This includes the contributions from the LGAD, the preamplifier-discriminator-TDC chain and the time walk correction, as well as from the beam telescope system clock distribution and the ETROC1 internal H-tree clock distribution. One of the main focus of the ETROC2 design is to minimize the 40MHz noise based on what has been learned from ETROC1, in order to lower the discriminator threshold to study the timing performance when LGAD gain is reduced due to irradiation towards the end of life at HL-LHC. The ETROC2 is the first full size (16x16) and full functionality prototype and its dimension is 21mm x 23mm making it one of the largest chips in HEP. The pixel analog front-end design is based on the ETROC1 pixel design, while the pixel readout and global readout design is entirely new with a switch-cell based network approach. A few new features have been added to the ETROC2, including the on-chip auto discriminator threshold calibration, built-in self-testing capability with digital pattern generation, as well as the capability to provide a coarse map of delayed hits continuously for every bunch crossing for monitoring or Level 1 triggering purposes. To minimize the risk from ETROC1 to ETROC2, a few dedicated testing chips were designed and carefully tested, including the rad-hard version of the waveform sampler chip, the ETROC-PLL chip which is based on the lpGBT PLL, and special I2C testing chip. In addition, the new pixel and global readout has been emulated in FPGA for design verification and testing purposes. In this presentation, the

most recent new ETROC1 beam test results and the test results of the new testing chips will be summarized, and the main ETROC2 design features will be presented as well.

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