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Results with the TOFHIR2B revision of the front-end ASIC of the CMS MTD Barrel Timing Layer

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The CMS Detector will be upgraded for the HL-LHC to include a MIP Timing Detector (MTD), which will consist of barrel and endcap timing layers, BTL and ETL. The BTL sensors are based on LYSO:Ce scintillation crystals coupled to SiPMs read-out by TOFHIR2 ASICs in the front-end system. A resolution of 30 ps for MIP signals is expected at the beginning of HL-LHC operation, degrading to 60 ps at the end of operation due to SiPMs radiation damage.
We present an overview of the TOFHIR2 requirements and design, and the recent results of the measurements with its final version, TOFHIR2B.

Summary (500 words)

The Phase II Upgrade Program of the CMS experiment at CERN's Large Hadron Collider includes the construction of a new MIP Timing Detector to measure the time of charged particles with high precision [1]. In the barrel section, the Barrel Timing Layer (BTL) is a thin standalone detector based on scintillation LYSO:Ce crystals bars read-out on both ends with silicon photomultipliers (SiPMs). The full BTL detector has about 330 thousand SiPM channels. The readout of the SiPMs uses the new TOFHIR2 chip [2].

The main requirements for the BTL electronics are: (1) to measure the timing of minimum ionizing particles (MIP) with a precision of 30 (60) ps at the beginning (end) of HL- LHC; (2) and to provide a measurement of the signal amplitude with <5% precision for time-walk corrections. Additionally, the chip has to cope with a MIP input rate of 2.5 M hit/s, to have an output bandwidth of 640 Mb/s, and to have a static power consumption lower than 15 mW per channel.
A summary of the TOFHIR2 specification parameters is given in Table I. The ASIC has 32 channels. A block diagram of one TOFHIR2 channel is shown in Fig. 1.Each ASIC channel contains independent amplifiers, leading edge discriminators, time-to-digital converters, charge-to-digital converters, a 40MHz 10-bit SAR ADC and local control logic.
In TOFHIR2, pulse filtering is included in the post-amplifiers to mitigate the deterioration of time resolution due to the large DCR induced by radiation (up to 55 GHz) and due to pile-up of LYSO pulse tails.
Two output data links each running at 320 Mb/s provide the required bandwidth. Four input links at 80 Mb/s are used for configuration, external triggering, synchronization and test pulse input. The clock frequency is 160 MHz. TOFHIR2 includes two 8-bit DACs to adjust the two SiPM bias voltages provided by the ALDO2 chip [3].
Relative to the first version of the front-end ASIC (TOFHIR2A), the second version, TOFHIR2X, implements improved circuitry for mitigation of the SiPM dark count noise (DCR) as well as a new current mode discriminator. The final version, TOFHIR2B, implements a new baseline holder circuit, a configurable baseline in the pulse charge integration allowing to optimize the dynamic range, and a tunable amplification gain to maintain the signal/noise performance in scenarios with SiPM pulses smaller than in the design version.

The measured performances of TOFHIR2A and TOFHIR2X match well the simulation expectations [4,5]. Successful TID and SEU radiation tests have been performed. The time resolution measured with the TOFHIR2X version is ˜25 ps (˜55 ps) at the beginning (end) of HL- LHC, assuming 30 GHz DCR at the end-of-life achievable by operating the SiPMs at -45oC with the help of Thermo-Electric Coolers.
The final prototype version of the ASIC, TOFHIR2B, is currently under test. The first results on the charge

integration performance of the improved QAC is shown in Fig. 2. At the conference, the measurements with TOFHIR2B, associated to prototype LYSO/SiPM sensors, will be presented.

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