TDC with Uncontrolled Delay Lines: Calibration Approaches and Precision Improvement Methods

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ABSTRACT: The time-to-digital-converter (TDC) using uncontrolled delay lines has a simple structure and finer measurement precision since the delay cells are pure digital gates that operate at maximum speed. For every incoming hit, two "snapshots" of the delay line are taken by the register array with two strobes separated with a known time interval. With two measurements, propagation delays of each cell in the delay line can be calibrated for the operating temperature and voltage. The two measurements can also be averaged to improve the TDC measurement precision. We will discuss various calibration approaches and present test results in this work.

KEYWORDS: Front-end electronics for detector readout; Solid state detectors; Timing detectors

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Contents

1. Introduction

The time-to-digital-converter (TDC) for the Endcap Layer Readout Chip (ETROC) in the CMS Endcap Timing Layer uses a scheme with uncontrolled delay lines. The propagation delay of each delay cell is not known and may vary at different temperatures and power supply voltages. Instead of "starving" the delay cells to slow them down to a given propagation delay, we let them operate at their maximum speed and measure the actual propagation delays during operation. Furthermore, we tolerate uneven timing bin widths so that a delay cell can be simply implemented with a single NAND gate which results in about an half of the propagation delay comparing with adding an inverter to change the polarity back, which otherwise we would have to do. In our test ASIC (ETROC1) at 65 nm technology, we have reached a nominal timing bin width of 17.8 ps with plain delay line without needing special structures such as vernier delay lines.

To measure or calibrate the actual propagation delays of the delay cells during operation, we use two strobes (separated by 3.125 ns in our case) to capture two "snapshots" of the delay line by the register array while the incoming hit is propagating in the delay line. The number of taps that the incoming signal flies through during the 3.125 ns reflects the average speed of the delay cells at the temperature and power supply voltage during operation. In the applications when the required measurement precision is not too fine so that the errors caused by the differential non-linearity are acceptable, a simple calibration based on the average bin width will produce satisfactory results, as shown in our previous work (about 10 ps standard deviation).

To further eliminate errors caused by the uneven timing bin width, we need to measure and maintain a bin-by-bin calibration lookup table before the measurement operation (and need to periodically update the lookup table during the gaps between the operations.) We used shifting phase clocks to produce the lookup table. The TDC is driven by a 40 MHz system clock while the incoming test hits are generated with a 40.001 MHz clock so that the incoming signals smear over the system clock period with steps as small as 0.625 ps. With bin-by-bin calibration, we have reached the TDC measurement precision better than 6 ps (std. dev.).

Once the calibration process is completed, the two measurements for an incoming hit can be averaged for even finer measurement precision. Our test results show that with the bin-by-bin

calibration applied to the two measurements and making arithmetic average, the TDC measurement precision improved from better than 6 ps to better than 5 ps.

Tests are made at both room temperature (about 25 C) and a high temperature (about 40 C) and the bin-by-bin calibration processes produce expected results in both cases. Our test results further show that the calibration table created at one temperature can be utilized at another temperature with appropriate scaling using the two measurements with double strobe.

In Section 2, we describe a few calibration approaches used in our work. Section 3 presents test results followed by conclusions in Section 4.

2. Delay line calibration approaches

The TDC implemented in ETROC ASIC uses 63 NAND gates to form a delay line as shown in Figure 1. The propagation delays of the NAND gates are not controlled for simplicity and their delays can be changed slowly with temperature and power supply voltage.

When the TDC channel is in standby condition, the START signal is LO and therefore all the even indexed delay line taps: D0, D2, ... D62 are in HI logic level while all odd indexed taps: D1, D3, ... D61 are in LO level. When the input signal arrives, the START signal turns to HI and a logic transition is propagating inside the delay line. More specifically, D0 turns from HI to LO, followed by D1 turns from LO to HI and so on. The output of D62 is routed back to the first NAND gate to extend the measurement range. Two arrays of registers are used to capture the time of arrival (TOA) of the START signal relative to the system clock and the time over threshold (TOT) of the incoming pulse.

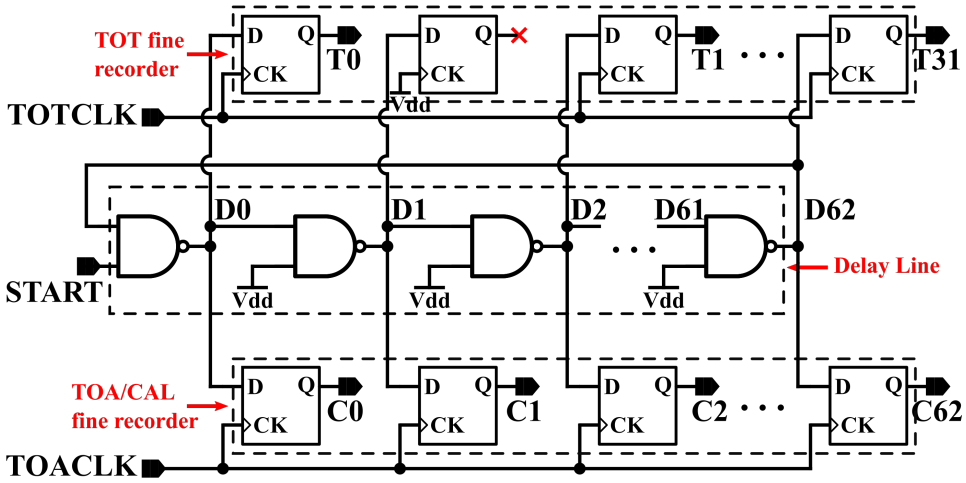

Figure 1. Simplified block diagram of an ETROC TDC channel

Since the propagation delays of the NAND gates are not controlled, they must be measured during operation. We use the double strobe approach to measure the average propagation delay as shown in Figure 2 which is the starting point of various calibration approached.

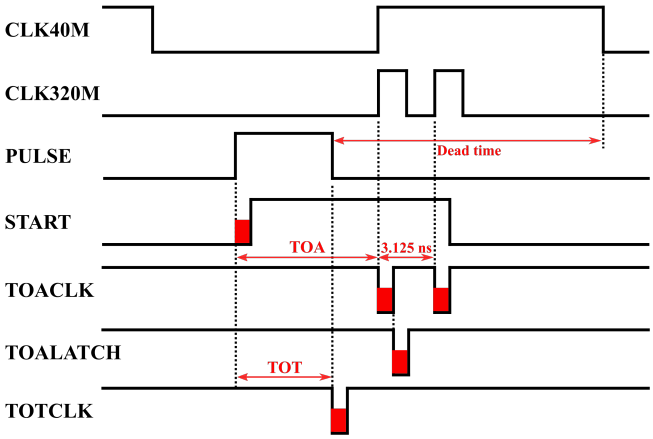

Figure 2. Timing diagram of the ETROC TDC operation

The TDC is driven by a 40 MHz system clock CLK40M and a 320 MHz clock is generated in the phase-lock-loop PLL block inside the ASIC. When an incoming pulse arrives, the START signal turns on and two strobes are enabled on the TOACLK which are derived from the 320 MHz clock. The separation of the strobes can be chosen to be integer multiples of the 320 MHz clock period, 3.125 ns. If the logic transition at N1 is captured by the first strobe and N2 by the second strobe, obviously, the average propagation delay of the NAND gates is 3125/(N2-N1) ps.

However, even in a carefully designed ASIC, it is difficult to achieve uniform propagation delays for all delay cells. Especially when we use single NAND gates as delay cells allowing both LO to HI and HI to LO transitions in the delay line, the even and odd taps would naturally exhibit alternating narrow-wide bin width variations. To eliminate measurement errors due to different bin widths, we used shifting phase clocks to measure the bin widths and produce the calibration lookup tables. The TDC is driven by a 40 MHz system clock while the incoming test hits are generated with a 40.001 MHz clock so that the incoming signals smear over the system clock period with steps as small as 0.625 ps. The measured bin widths of some TDC codes are shown in Figure 3.

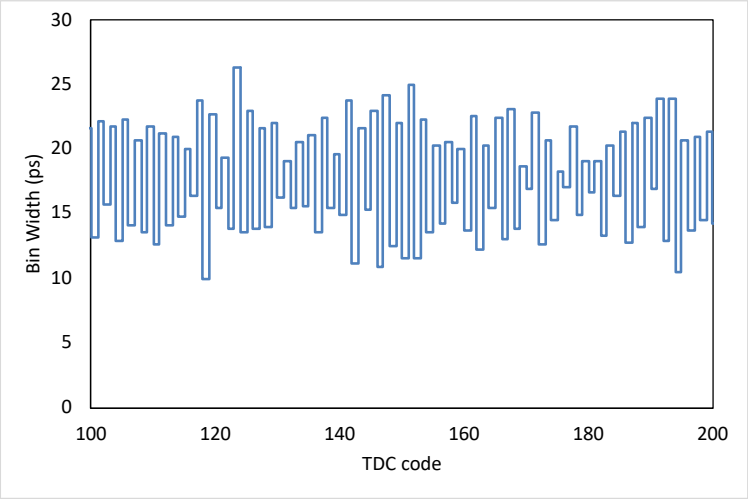

Figure 3. Bin widths for some TDC codes

The bin widths of the TDC codes are accumulated together to create a lookup table which converts TDC code to measured signal arrival time in unit of picoseconds. A lookup table at certain temperature and power supply voltage created using test data is plotted in Figure 4, in which TOA0 and TOA1 are two measurements with the two strobes described earlier.

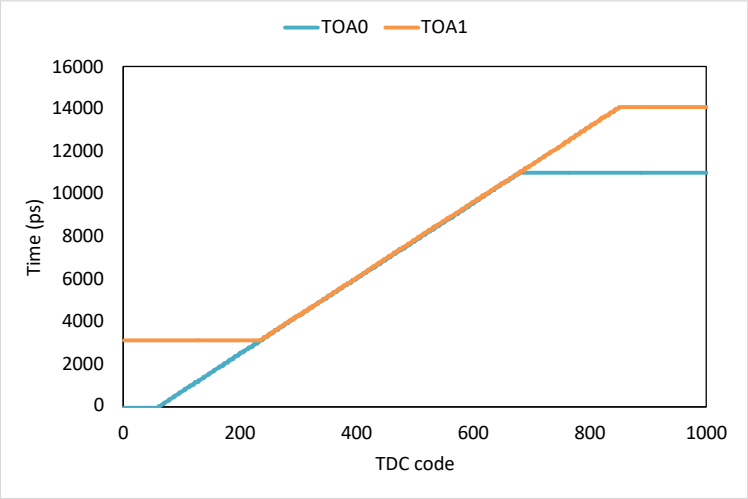

Figure 4. Calibration lookup table of a ETROC TDC at an operating condition

With calibration lookup table, errors caused uneven bin widths can be eliminated using bin-by-bin calibration.

It should be pointed out that ideally the lookup table should be updated frequently to accommodate temperature variation of during the operation. However, in some circumstances, it may not be convenient to update the lookup table as often as users want. To solve this problem, it is possible to use lookup table produced at different temperature with appropriate scaling using information based on TOA0 and TOA1.

3. Test results

This section presents test results of an ETROC TDC measured at two different temperatures.

3.1 Temperature variations and effects of bin-by-bin calibration

Measurements are performed on an ETROC TDC at two different temperatures, one at room temperature (about 25 degree C) and another at a higher temperature (heated with a hot air gun to about 40 degree C). The test setup operated at a system clock of 40 MHz and the input test signals are generated with a 40.001MHz clock so that the phase shift relatives to the system clock between test signals are known and smears over entire range of system clock period (25 ns).

A very notable phenomenon is the shift of the calibration code, TOA1-TOA0. At the room temperature, the typical calibration codes are about 174 as shown by the right peak in top histogram in Figure 4. At higher temperature, the calibration code shifted to about 171 as shown by the left peak.

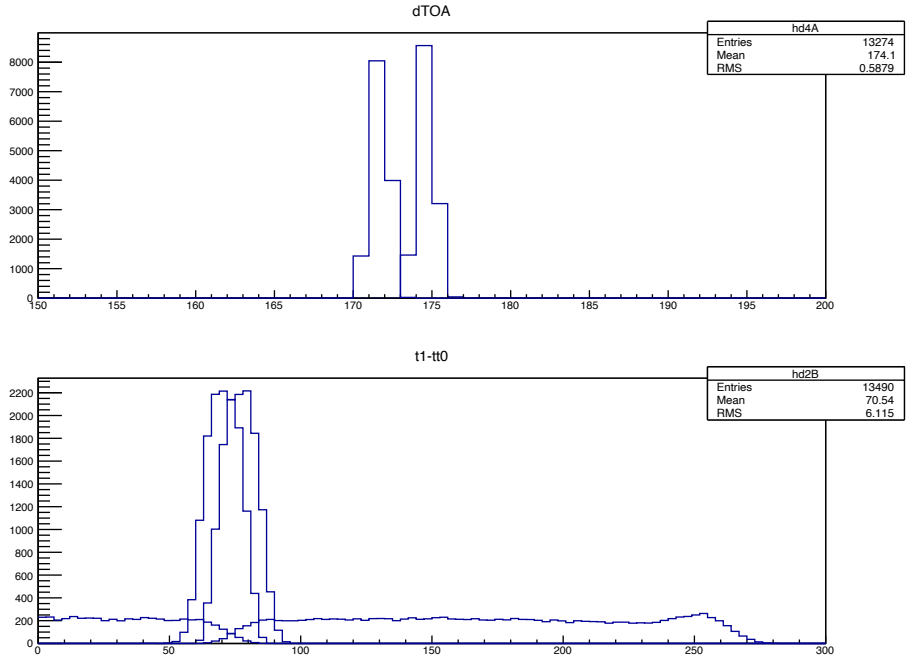

Figure 5. Calibration codes and calibrated times at different temperatures

The differences of measured times and the known arrival times of the test signals are plotted in the lower histogram in Figure 4. The two peaks in the histogram represent measurements at two different temperatures. The raw TDC codes from the measurements are converted to calibrated time using the lookup table. The data from two temperatures are calibrated using opposite lookup tables, meaning that the low temperature data are calibrated with lookup table produced at high temperature and vise versa. However, the calibrate table are rescaled using (TOA1-TOA0)$_{\{\text{current temperature}\}}$/(TOA1-TOA0) $_{\{\text{lookup table temperature}\}}$. As it is shown in the histogram, the standard deviation of the difference between measured time and the known time is typically 6 ps if the bin-by-bin calibration is applied with appropriate temperature scaling.

If the temperature scaling is not used, the difference between measured time and the known time would spread over large range, as the two flat curves plotted in the histogram above.

3.2 Improving measurement precision using the double strobe data

The TOA0 and TOA1 are two measurements in the same delay line with a known timing separation (3.125 ns in our case). The primary purpose of making two measurements is to monitor and calibrate temperature variations. Since the temperature of the silicon substrate usually does not change very rapidly, therefore, after calibration, these two measurements can also be used to improve the measurement precision.

The differences between measured times and the known times with bin-by-bin calibration and temperature scaling are plotted in the top histogram in Figure 5. The left peak represents TOA0 while the right peak represents TOA1. (Since TOA1 is 3125 ps larger than TOA0 for a same hit, a 3000 ps constant is subtracted from TOA1 so that it can be shown in the same plot with TOA0) Typical standard deviation in this situation is about 6 ps.

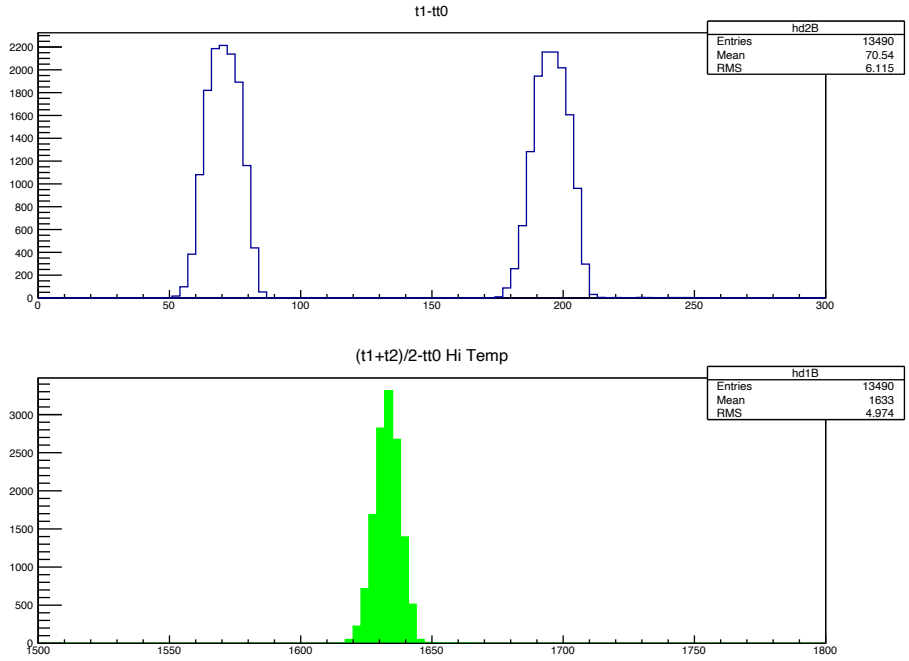

Figure 6. Block diagram of ETROC with the single pixel channel in detail.

When an arithmetic average ($t_{TOA1}+t_{TOA0}$)/2 is calculate for each hit, the standard deviation improves to better than 5 ps, as shown in the lower histogram in Figure 5.

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4. Conclusion

This paper presents serval calibration approaches for a TDC with uncontrolled delay line. Our tests show that the TDC in the ETROC ASIC functions as expected and is able to accommodate variations of the temperature and maintains fine measurement precisions. Also, advantages can be taken to further improve measurement precisions using the two measurements collected with double strobe.

ETROC2, the next iteration of the ETROC series, will contain the full functionality by using the full 16×16 pixel matrix. The proposed threshold calibration circuit will be implemented inside each pixel in ETROC2. Full data readout chain will be designed, implemented and tested.

Acknowledgments

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