Contribution ID: **139** Type: **Oral**

TDC with Uncontrolled Delay Lines: Calibration Approaches and Precision Improvement Methods

Thursday 22 September 2022 11:20 (20 minutes)

The time-to-digital-converter (TDC) using uncontrolled delay lines has a simple structure and finer measurement precision since the delay cells are pure digital gates that operate at maximum speed. For every incoming hit, two "snapshots" of the delay line are taken by the register array with two strobes separated with a known time interval. With two measurements, propagation delays of each cell in the delay line can be calibrated for the operating temperature and voltage. The two measurements can also be averaged to improve the TDC measurement precision. We will discuss various calibration approaches and present test results in this work.

Summary (500 words)

The time-to-digital-converter (TDC) for the Endcap Layer Readout Chip (ETROC) in the CMS Endcap Timing Layer uses a scheme with uncontrolled delay lines. The propagation delay of each delay cell is not known and may vary at different temperatures and power supply voltages. Instead of "starving" the delay cells to slow them down to a given propagation delay, we let them operate at their maximum speed and measure the actual propagation delays during operation. Furthermore, we tolerate uneven timing bin widths so that a delay cell can be simply implemented with a single NAND gate which results in about an half of the propagation delay comparing with adding an inverter to change the polarity back, which otherwise we would have to do. In our test ASIC (ETROC1) at 65 nm technology, we have reached a nominal timing bin width of 17.8 ps with plain delay line without needing special structures such as vernier delay lines.

To measure or calibrate the actual propagation delays of the delay cells during operation, we use two strobes (separated by 3.125 ns in our case) to capture two "snapshots" of the delay line by the register array while the incoming hit is propagating in the delay line. The number of taps that the incoming signal flies through during the 3.125 ns reflects the average speed of the delay cells at the temperature and power supply voltage during operation. In the applications when the required measurement precision is not too fine so that the errors caused by the differential non-linearity are acceptable, a simple calibration based on the average bin width will produce satisfactory results, as shown in our previous work (about 10 ps standard deviation).

To further eliminate errors caused by the uneven timing bin width, we need to measure and maintain a bin-by-bin calibration lookup table before the measurement operation (and need to periodically update the lookup table during the gaps between the operations.) We used shifting phase clocks to produce the lookup table. The TDC is driven by a 40 MHz system clock while the incoming test hits are generated with a 40.001 MHz clock so that the incoming signals smear over the system clock period with steps as small as 0.625 ps. With bin-by-bin calibration, we have reached the TDC measurement precision better than 6 ps (std. dev.).

Once the calibration process is completed, the two measurements for a incoming hit can be averaged for even finer measurement precision. Our test results show that with the bin-by-bin calibration applied to the two measurements and making arithmetic average, the TDC measurement precision improved from better than 6 ps to better than 5 ps.

Tests are made at both room temperature (about 25 C) and a high temperature (about 40 C) and the bin-by-bin calibration processes produce expected results in both cases. Our test results further show that the calibration table created at one temperature can be utilized at another temperature with appropriate scaling using the

two measurements with double strobe.

Primary authors: LIU, Chonghan (S); EDWARDS, Chris (Fermi National Accelerator Lab. (US)); WU, Jinyuan (Fermi National Accelerator Lab. (US)); GONG, Datao (Southern Methodist Univeristy); SUN, Hanhan (Southern Methodist University); OLSEN, Jamieson (Fermi National Accelerator Lab. (US)); YE, Jingbo (Southern Methodist University (US)); ZHANG, Li; SUN, Quan (Fermi National Accelerator Lab.); LIU, Tiankuan (Southern Methodist University (US)); LIU, Tiehui Ted (Fermi National Accelerator Lab. (US)); ZHANG, Wei (Southern Methodist University); HUANG, Xing (Southern Methodist University)

Presenter: WU, Jinyuan (Fermi National Accelerator Lab. (US))

Session Classification: ASIC

Track Classification: ASIC