European Research Council
Established by the European Commission

Monolithic pixel sensor design for picosecond-level time resolution

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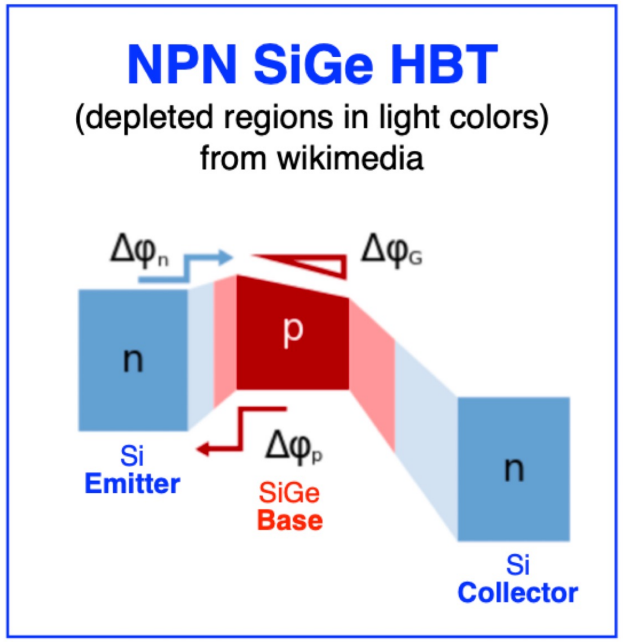
The MONOLITH ERC Project

Funded by the H2020 ERC Advanced grant 884447[1], July 2020 - June 2025

- **Monolithic silicon sensor** able to:
  - precisely measure 3D spatial position of charged particles
  - provide picosecond time resolution
- Technology choice:
  - Fast and low-noise **SiGe BiCMOS** electronics
  - Novel sensor concept: the **Picosecond Avalanche Detector (PicoAD)**

[1] MONOLITH H2020 ERC Advanced Project Web Page - https://www.unige.ch/dpnc/en/groups/giuseppe-iacobucci/research/monolith-erc-advanced-project/

Leading-edge technology IHP SG13G2, 130 nm IHP process featuring SiGe HBT



SiGe HBT = BJT with Germanium as base material:

- higher doping in base possible
- thinner base
- **reduced base resistance R_b**

Grading of Ge doping in base:

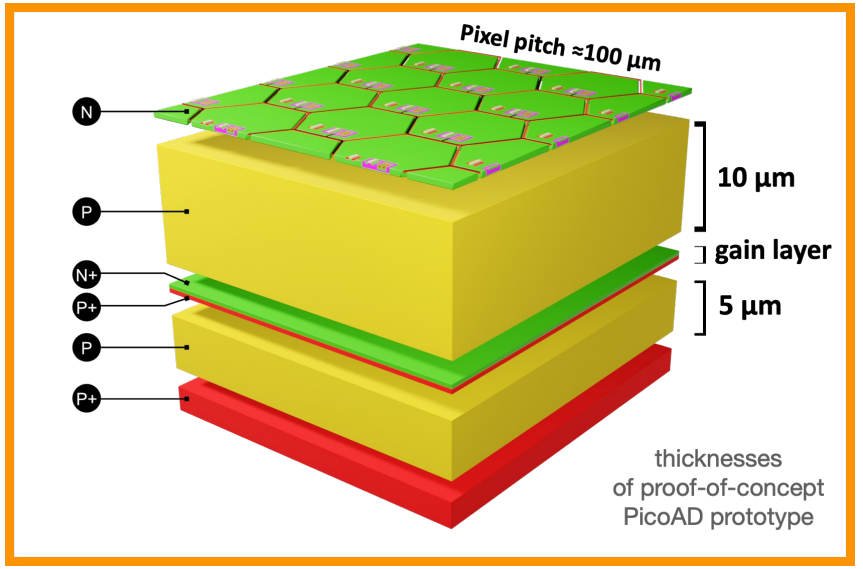
- charge transport in base via drift
- reduced charge transit time in base
- **high current gain β**

$$ENC_{series\ noise} \propto \sqrt{k_1 \frac{C^2_{tot}}{\beta} + k_2 R_b C^2_{tot}}$$

PicoAD I Sensor Concept

Multi-Junction Picosecond-Avalanche Detector[1]

- Continuous and deep gain layer
  - De-correlation from implant size/geometry
    - **high granularity and full fill factor** (high spatial resolution)
  - Only small fraction of charge gets amplified
    - **reduced charge-collection (Landau) noise** (enhance timing resolution)

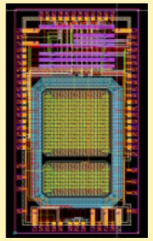


[1] G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector; European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018

SiGe BiCMOS prototypes at UniGe

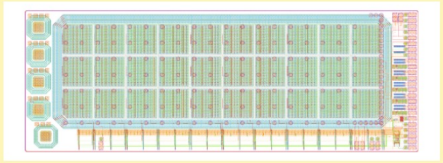
Prototypes without internal gain layer

2016



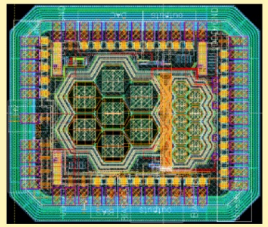
200ps
- 1 and 0.5 mm² pixels
- Discriminator output

2017



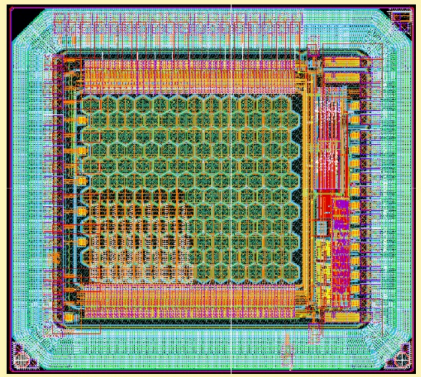
110ps
- 30 pixels 500x500µm²
- 100ps TDC +I/O logic

2018



50ps
- Hexagonal pixels 65µm and 130µm side
- Discriminator output

2019

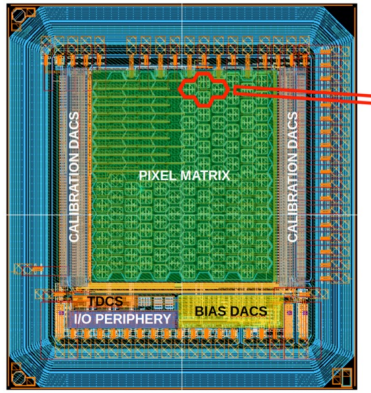


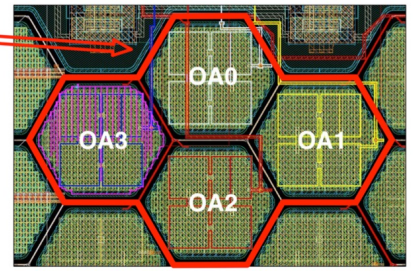
36 ps
- Hexagonal pixels 65µm side
- 30ps TDC +I/O logic
- Analog channels

Sensor with no gain test beam results: JINST **P02019** *2022*

PicoAD Proof-Of-Concept Prototype

2021

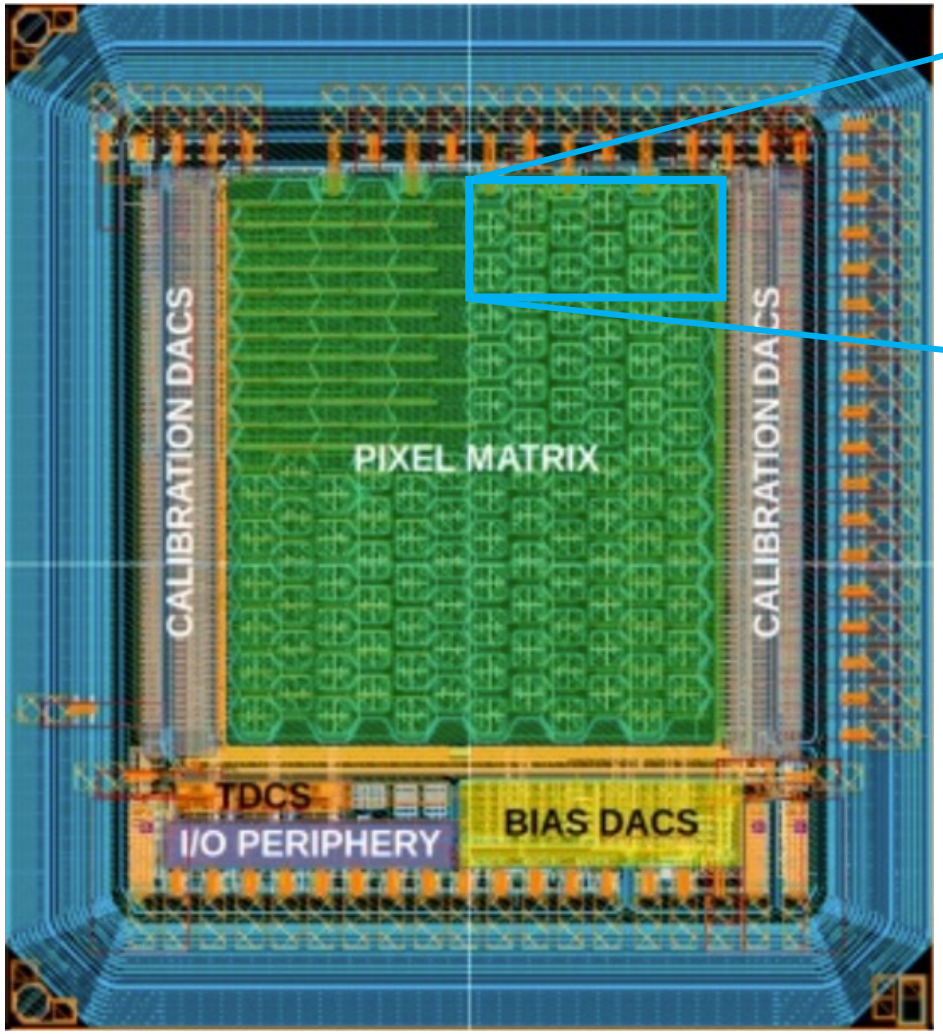


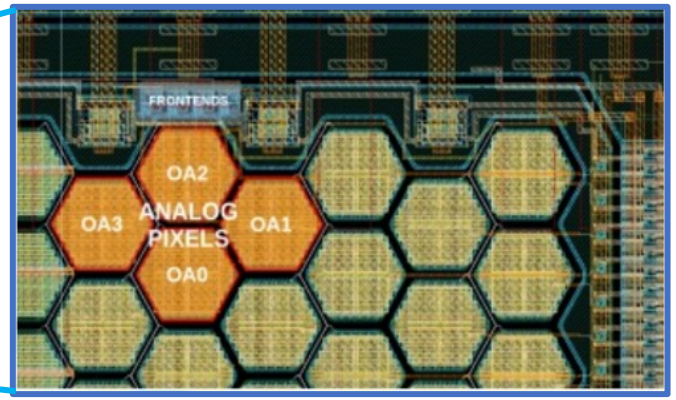


17 ps
- **Same electronics as 2019 prototype**
- **Epitaxial layers + gain layer**
- **4 different gain-layer doses**

PicoAD proof-of-concept prototype: arXiv:2206.07952, June 2022
Testbeam results: arXiv:2208.11019, August 2022

Analog pixels proof-of-concept prototype





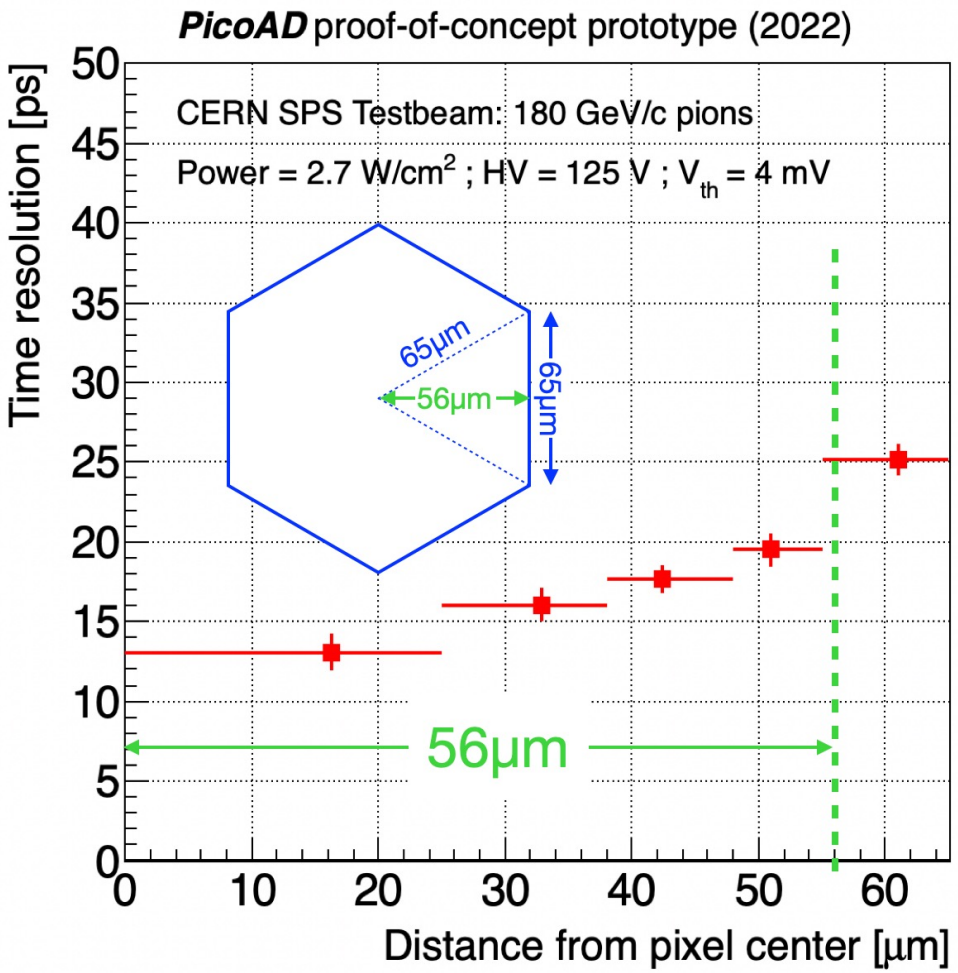
100 μm pitch hexagonal pixels
25 μm depletion

Front-end electronics:

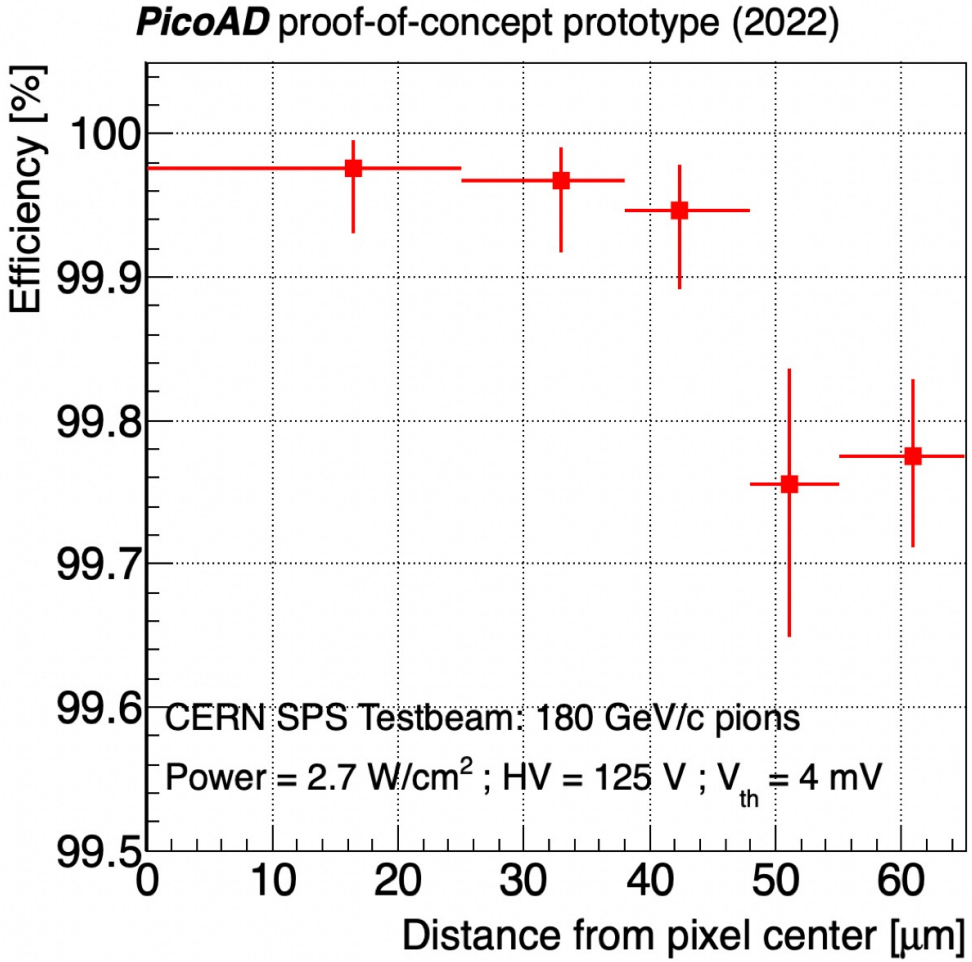
- HBT preamp (off-pixel)
- Two HBT BJT-based emitter follower (off-pixel) to drive 50 Ω

Testbeam results

Time resolution



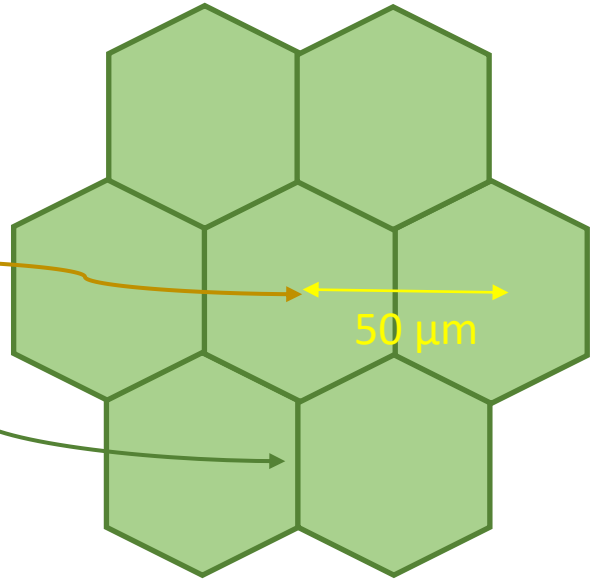
Efficiency



Next MONOLITH TESTCHIP

New prototype (submitted on September 16th)

- Proof of concept PicoAD prototype ⇒ time resolution ≈ 17 ps
- Next MONOLITH testchip ⇒ target time resolution ≤ 10 ps
  - PicoAD sensor
  - Improved electronics
  - Smaller capacitance: pixel pitch (112 μm → 50 μm)
  - Reduction of wells interpixel isolation gap (10 μm → 6 μm)

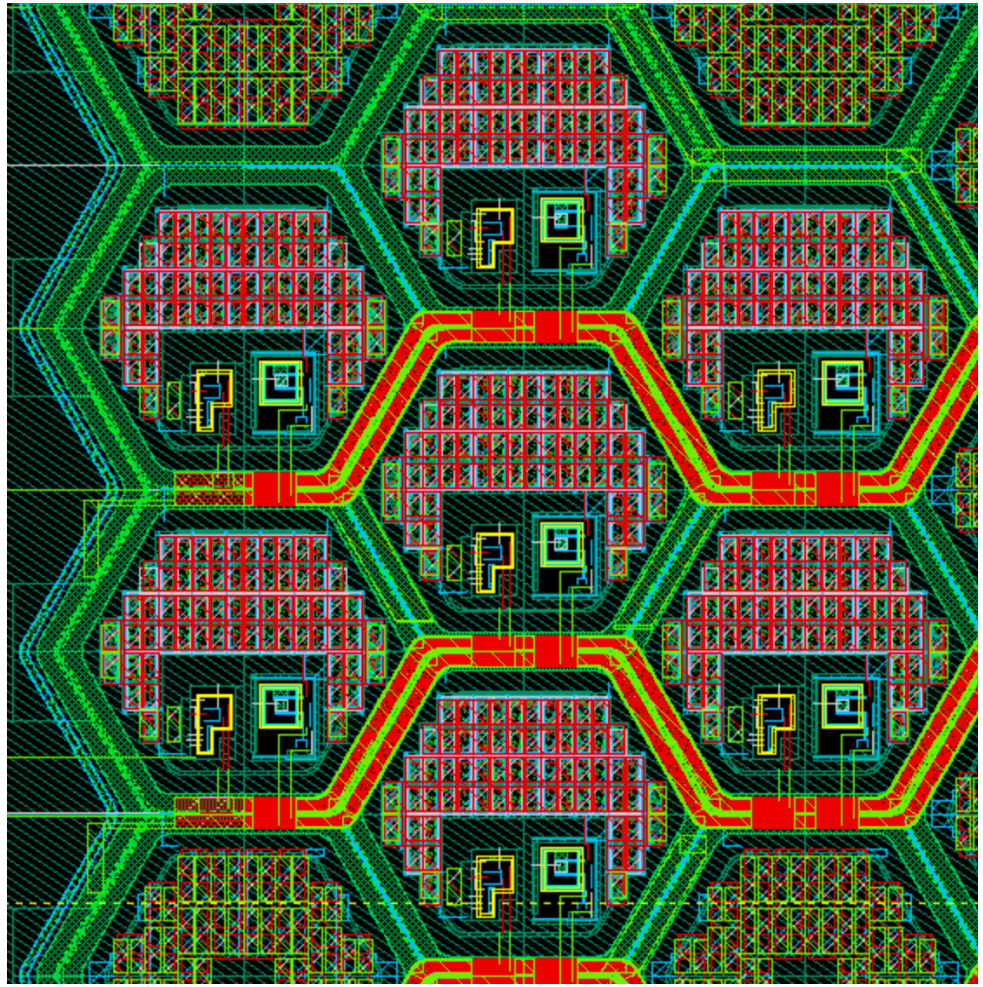


MONOLITH prototype I Flavors

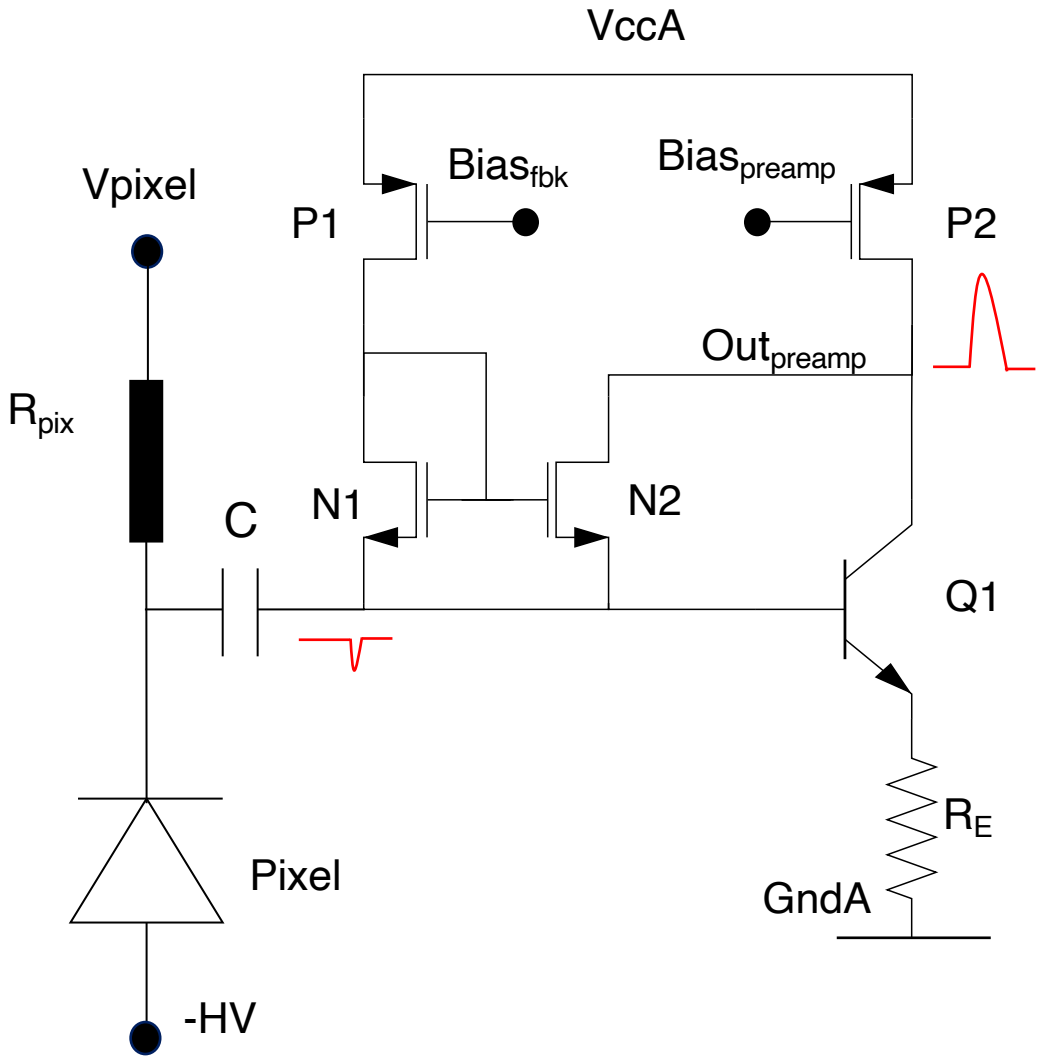
3 sub-matrices for probing performance of each stage of the FE architecture

Each sub-matrix with 7 analog pixels:

- **AM0:**
  - Preamp (in-pixel)
  - Driver stage (off-pixel)
- **AM1:**
  - Preamp (off-pixel)
  - Driver stage (off-pixel)
- **DM0:**
  - Preamp and Discriminator (in-pixel)
  - CML output



Preamp stage: how we improved it



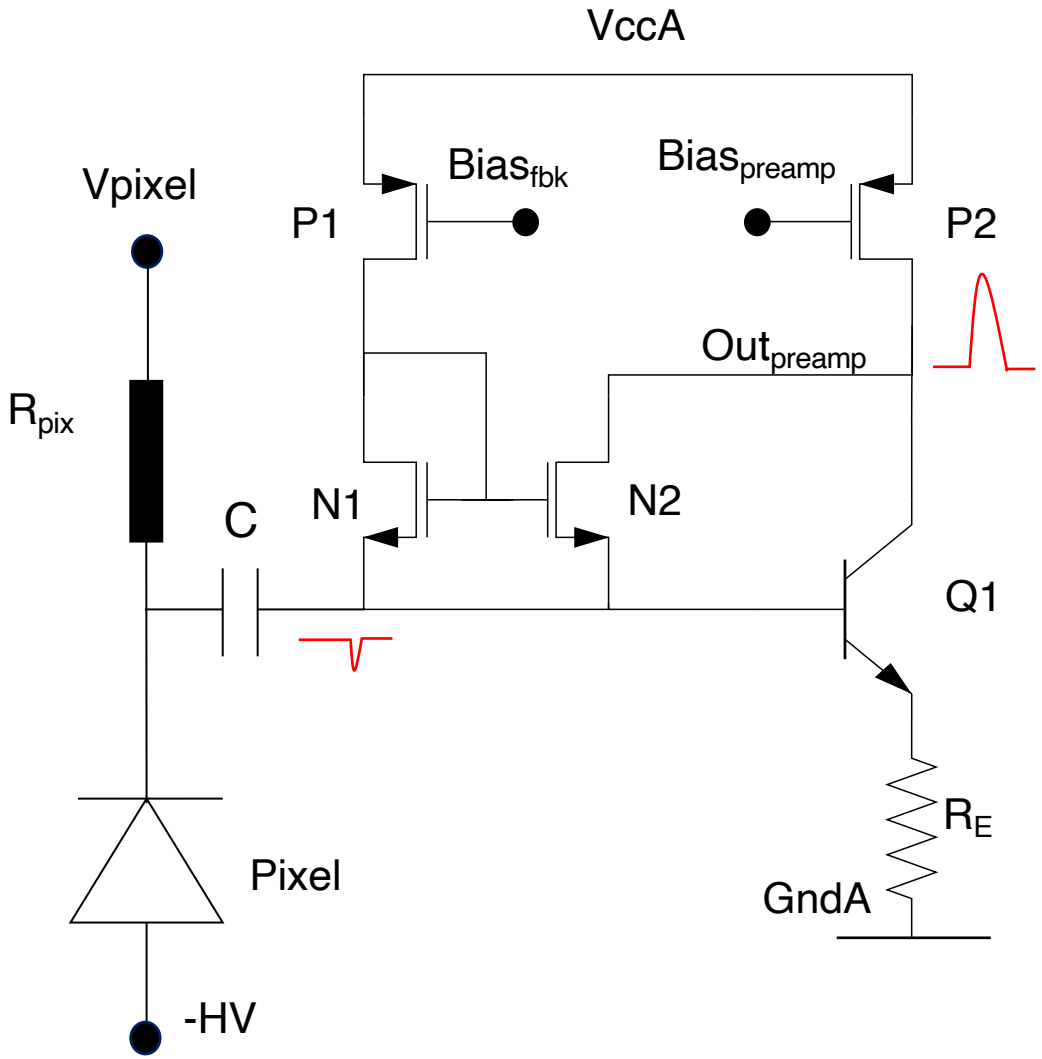
Charge sensitive amplifier:

- Single-ended BJT-based stage with **active load** (PMOS)
- Gain and BW controlled by Bias$_{fbk}$ (tunable feedback resistance)
- Preamp current set by Bias$_{preamp}$

Power consumption reduction:

- I_{preamp}: 150 μA → 50 μA
- V_{ccA} : 1.8 V → 1.2 V

Preamp contribution to jitter



Cadence Spectre simulation with:

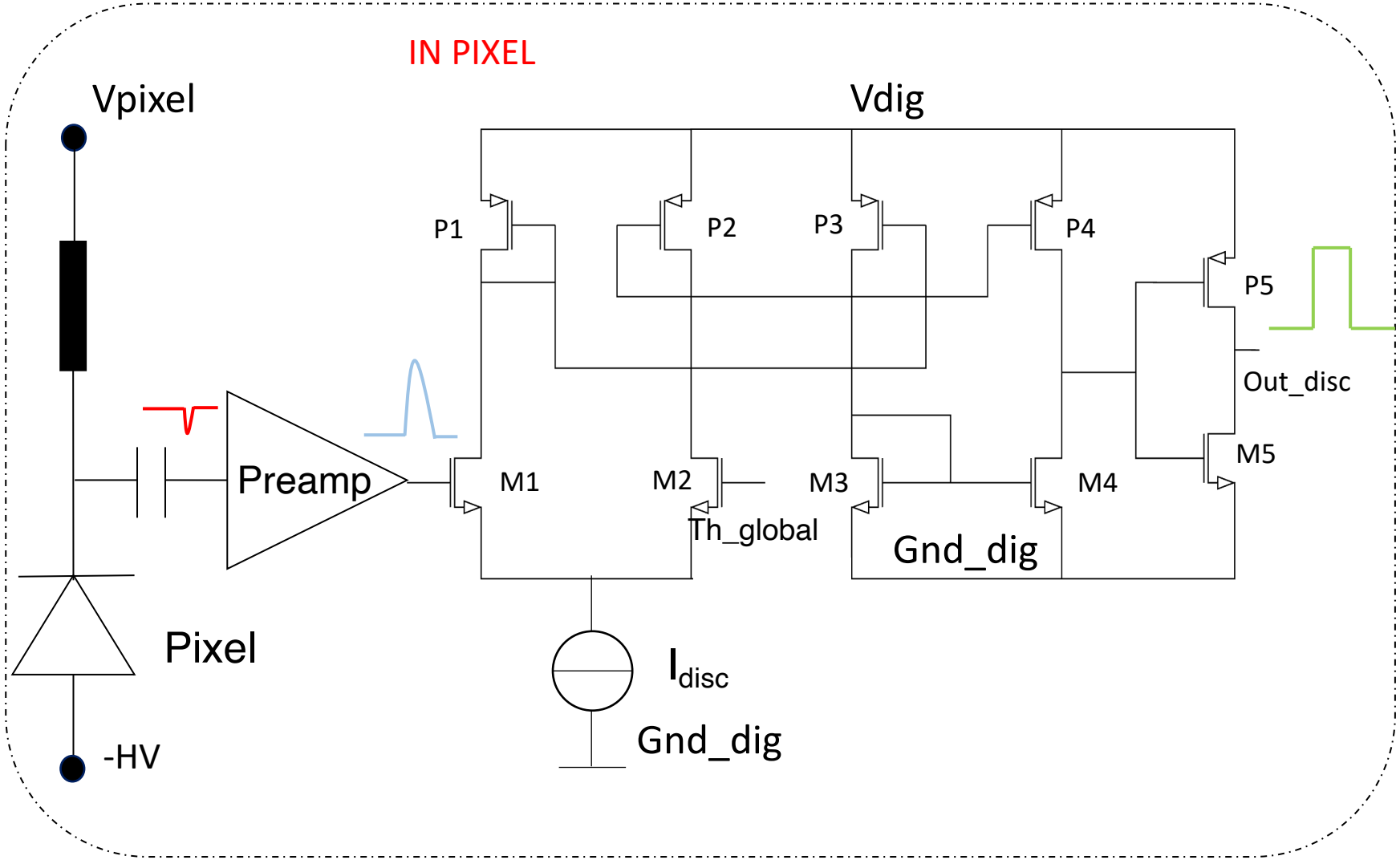
I_{fbk} = 10 nA I_{preamp}= 200 µA V_{ccA}= 1.2 V	I_{fbk} = 100 nA I_{preamp}= 50 µA V_{ccA}= 1.2 V

Component	Jitter$_{outPreamp}$ [ps]	Jitter$_{outPreamp}$ [ps]
BJT_hbt (Q1)	**6.9**	**3.4**
RE	2.3	1.8
Pmos_load (P2)	**4.8**	**3.1**
Nmos_fbk (N1) and (N2)	2.0	2.6
Pmos_fbk_slave (P1)	1.3	2.3
All_components	**8.7**	**4.4**

OLD DESIGN NEW DESIGN

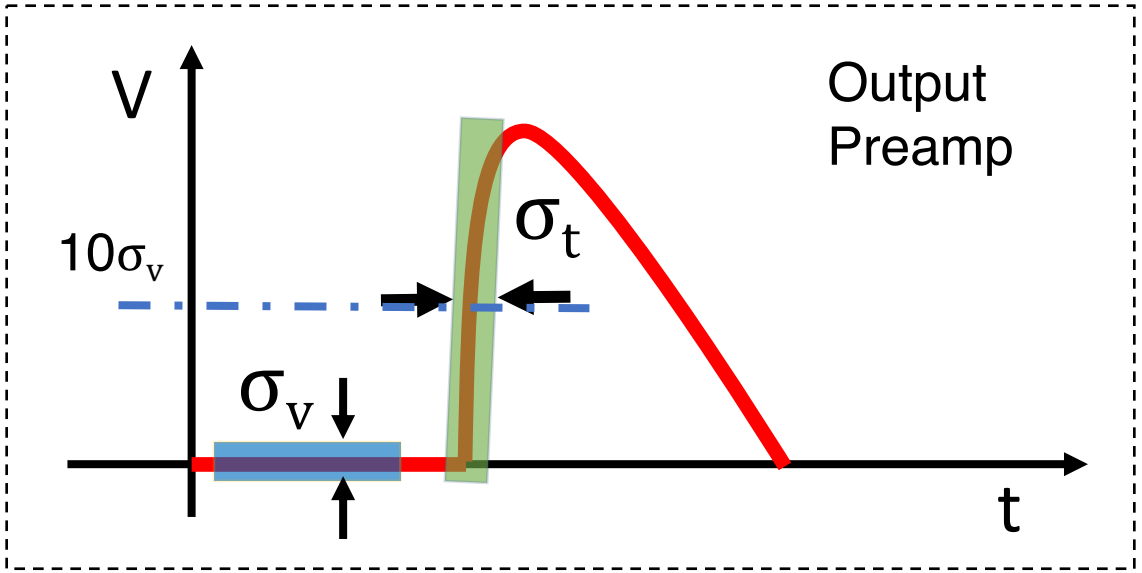
P2 and Q1 give the dominant contribute to the noise

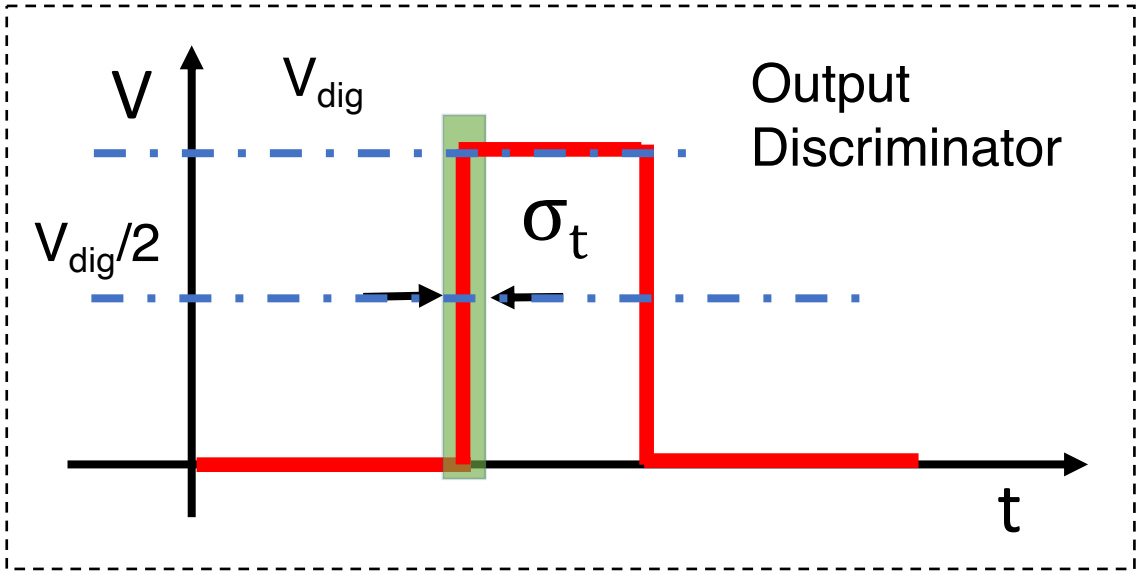
Discriminated Front-End (DM0)



- Same Preamp stage of analog matrices
- Fully differential:
  - Symmetrical input stage
- Discriminator design optimized for timing:
  - High gain
  - In-pixel integration
- Power consumption reduced
  - I_{disc}= 20 μA → 5 μA

Timing performance (simulated)





Cadence Spectre simulation for:

Input charge=1 fC

V_{ccA}=1.2 V I_{fbk}=100 nA I_{preamp}= 50 µA I_{disc} = 5 µA

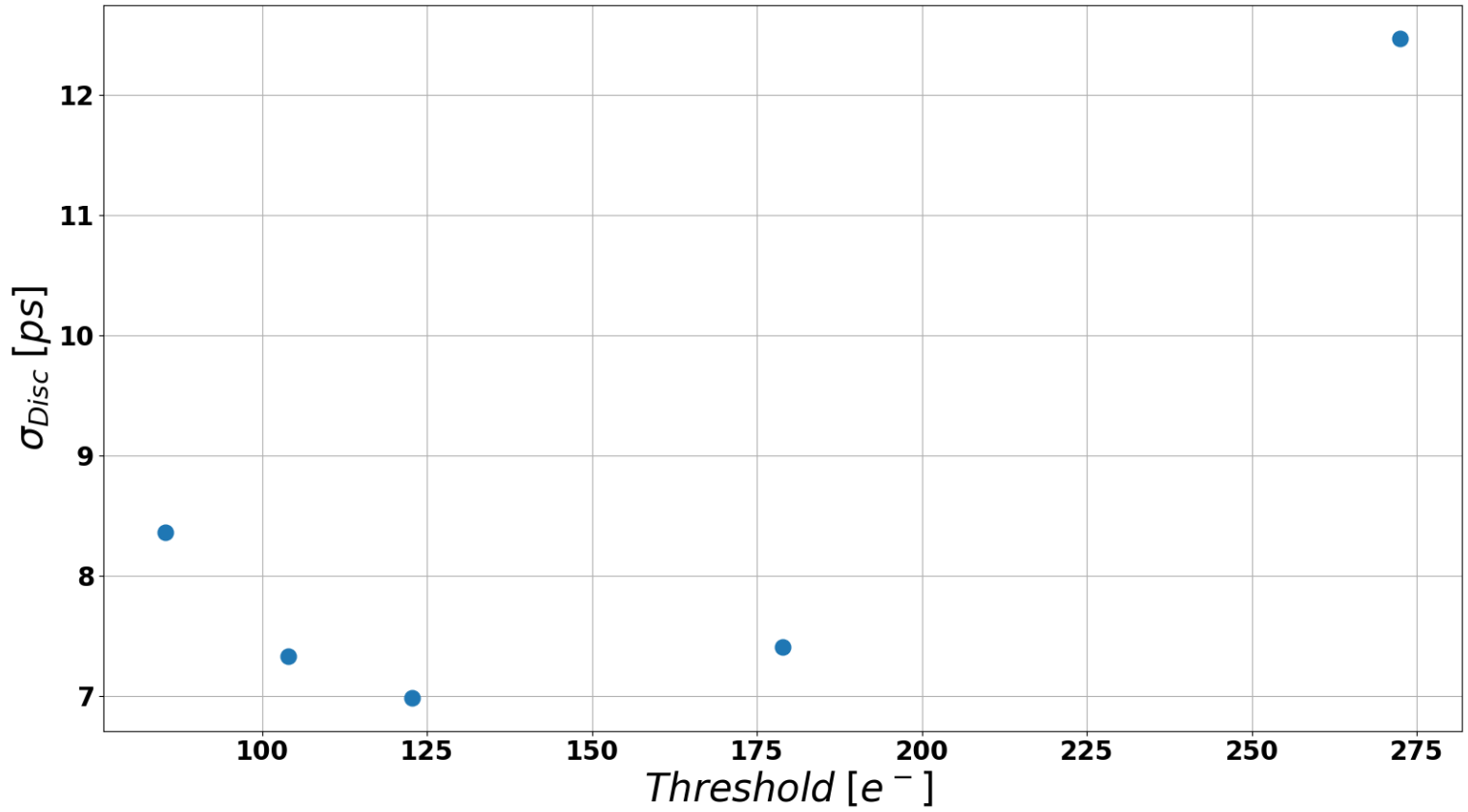
σ_{preamp}	$\sigma_{discriminator}$
≅5 ps	≅7 ps

DM0 timing performance with threshold scan

Cadence Spectre simulation

Input charge= 1 fC

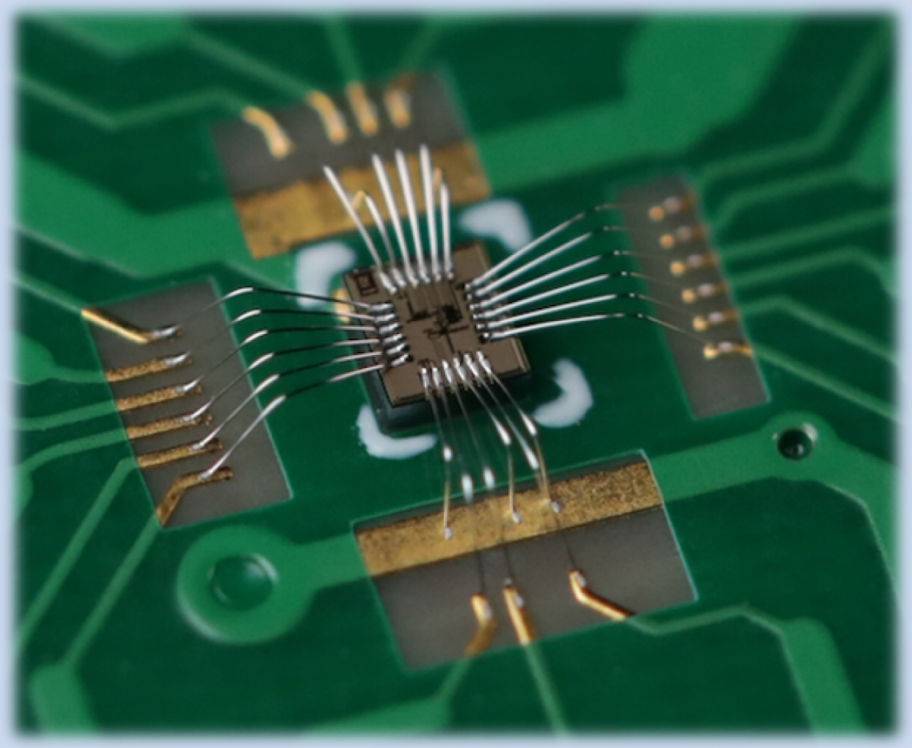
Ipreamp= 50 µA Ifbk= 100 nA VccA= 1.2 V Vdisc= 1.4 V Idisc= 5 µA

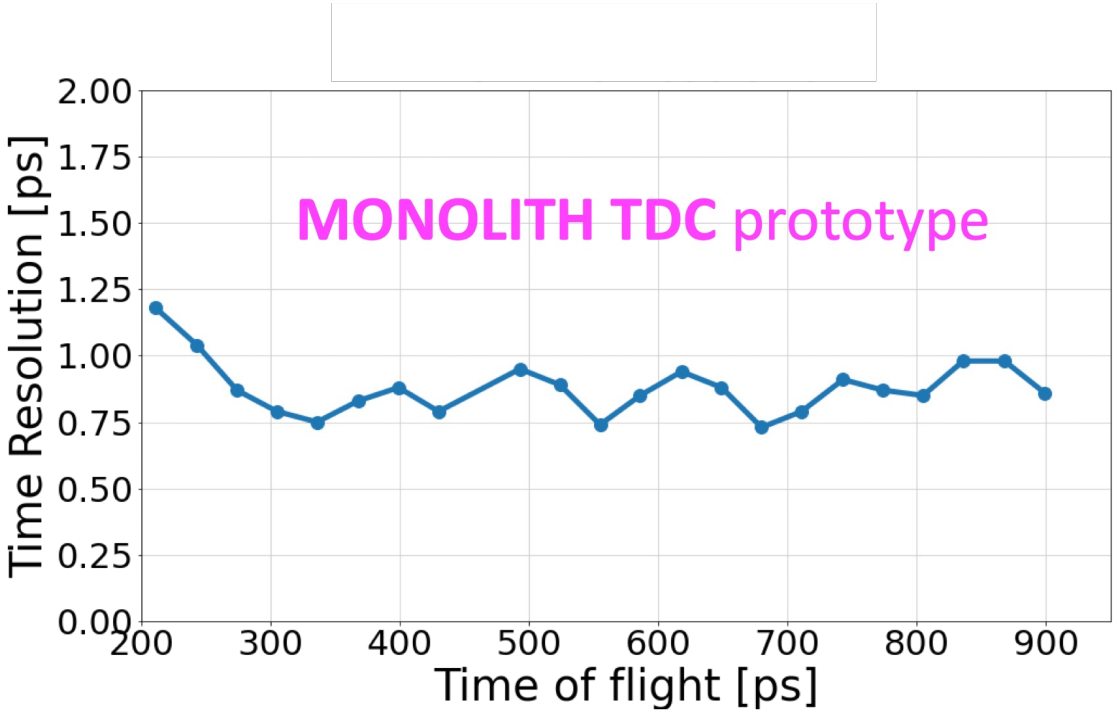


➢ At threshold around 125 e^-, σ_{Disc} below than 10 ps is obtained

Sub-picosecond TDC

We are developing a sub-picosecond TDC based on a novel design (our patent[5] & more):





Standalone prototype still under test at UNIGE.
Integrated in MONOLITH 2022 monolithic ASIC.

[5] R. Cardarelli, L. Paolozzi, P. Valerio and G. Iacobucci, European Patent Application / Filing - UGKP-P-001-EP, Europe Patent EP 18181123.3. 2 July 2018.

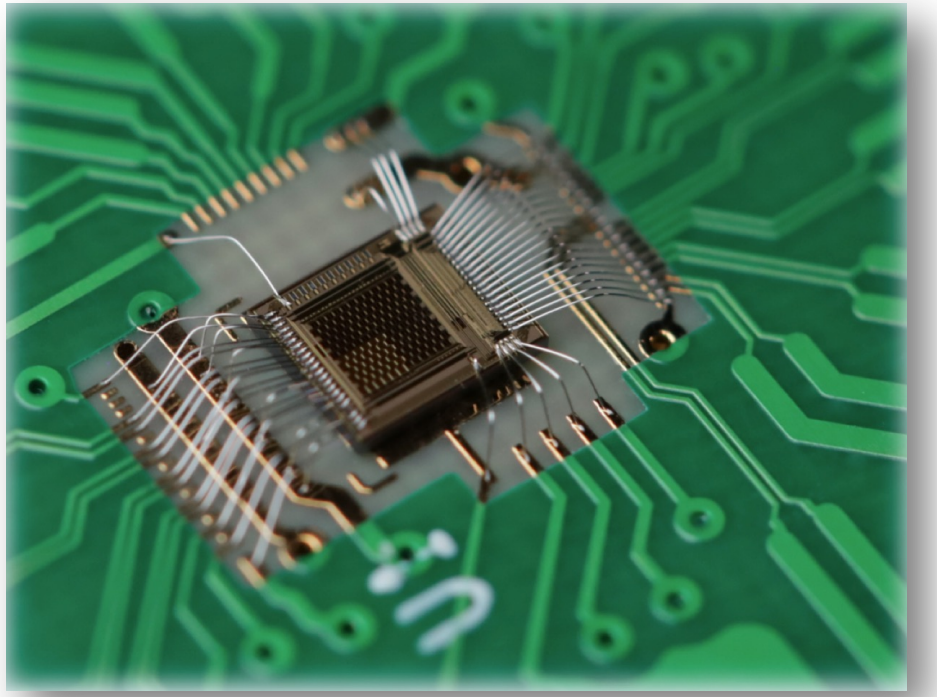
Summary

The PicoAD Monolithic proof-of-concept prototype

(100 μm pixel pitch, sensor not yet optimized for timing):

Full sensor-bias voltage:

- Efficiency= 99.9%
- Average Time resolution σ_t = (17.3 ± 0.4) ps



New ASIC monolithic prototype (just submitted) :

- 50 μm pitch and reduced interpixel distance
- Improved frontend
- New in-pixel discriminator

Full-reticle chip with 50 μm pitch and 10ps timing in Summer 2025

BACKUP SLIDES

MONOLITH TEAM

Giuseppe Iacobucci
- project P.I.
- System design

Thanushan Kugathasan
- Lead chip design
- Digital electronics

Roberto Cardella
- Sensor design
- Laboratory test

Mateus Vicente
- System integration
- Laboratory test

Matteo Milanesio
- Laboratory test
- Data analysis

Antonio Picardi
- Chip design
- Firmware

Jihad Saidi
- Laboratory test
- Data analysis

Carlo Alberto Fenoglio
- Chip design
- Firmware

Lorenzo Paolozzi
- Sensor design
- Analog electronics

Magdalena Munker
- Sensor design
- Laboratory test

Stefano Zambito
- Laboratory test
- Data analysis

Fulvio Martinelli
- Chip design
- Firmware

Théo Moretti
- Laboratory test
- Data analysis

Chiara Magliocca
- Laboratory test
- Data analysis

Rafaella Kotitsa
- Sensor simulation

Luca Iodice
- Chip design
- Firmware

Didier Ferrere
- System integration
- Laboratory test

Yannick Favre
- Board design
- RO system

Sergio Gonzalez-Sevilla
- System integration
- Laboratory test

Stéphane Débieux
- Board design
- RO system

Main research partners:

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INFN Rome2 & UNIGE

Holger Rücker
IHP Mikroelektronik

Marzio Nessi
CERN & UNIGE

Bernd Heinemann
IHP Mikroelektronik

Funded by:

Swiss National Science Foundation

European Research Council
Established by the European Commission

Sinergia

ATTRACT

UNIVERSITÉ DE GENÈVE | UNITEC

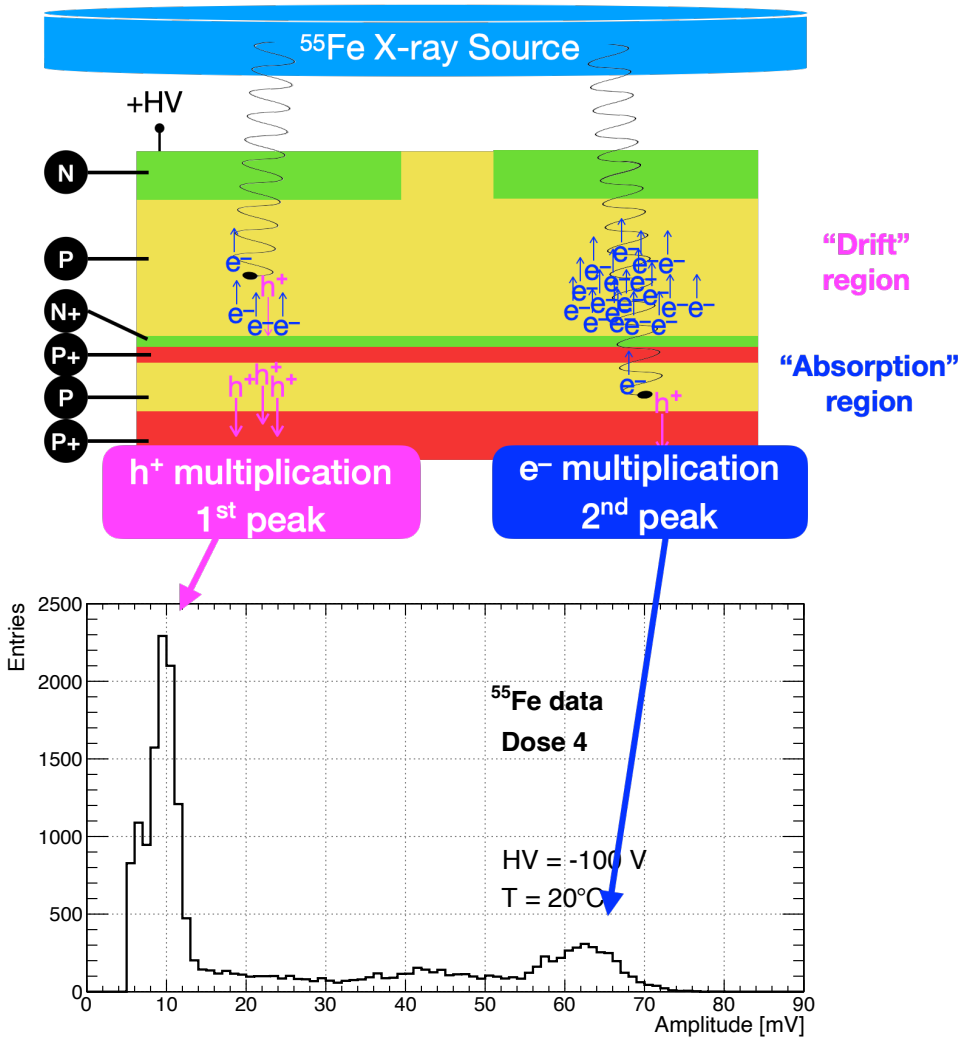
Gain measurements

X-rays from ^{55}Fe radioactive source:

- mainly ~5.9 keV photons
- point-like charge deposition

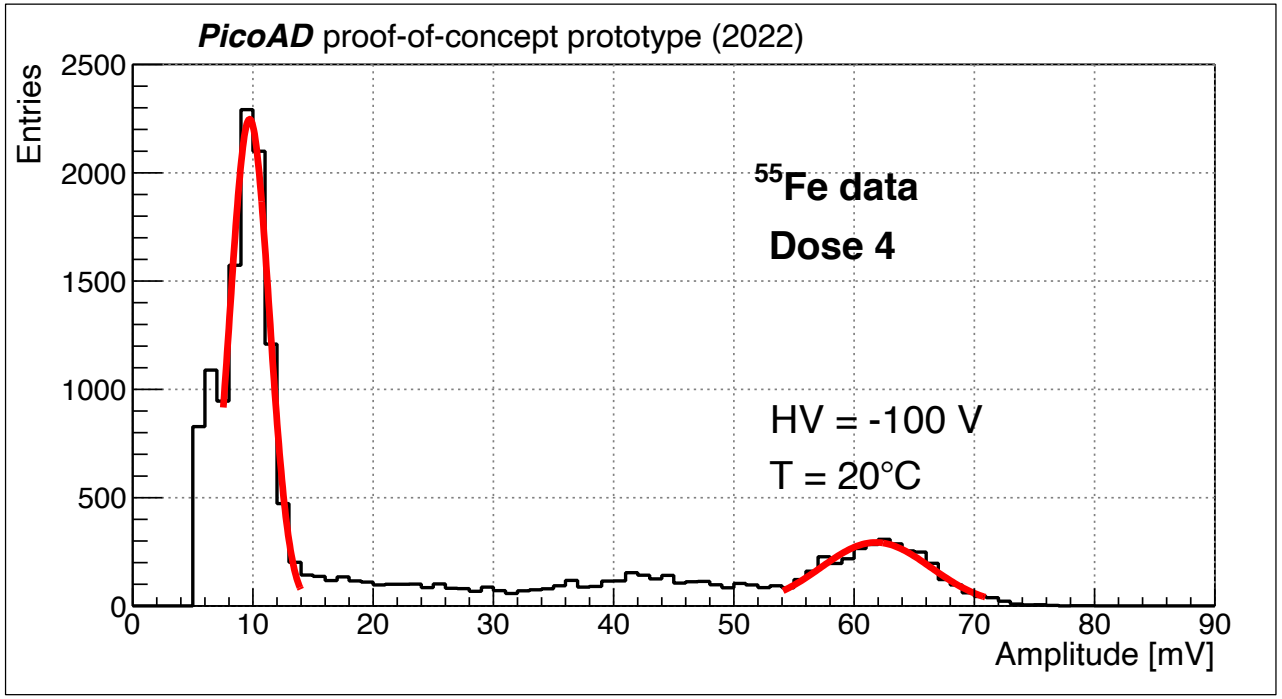
Characteristic double-peak spectrum

- photon absorbed in **drift region**
  - **holes** through gain layer & multiplied
  - **first peak** in the spectrum
- photon absorbed in **absorption region**
  - **electrons** though gain layer & multiplied
  - **second peak** in the spectrum



Gain measurements

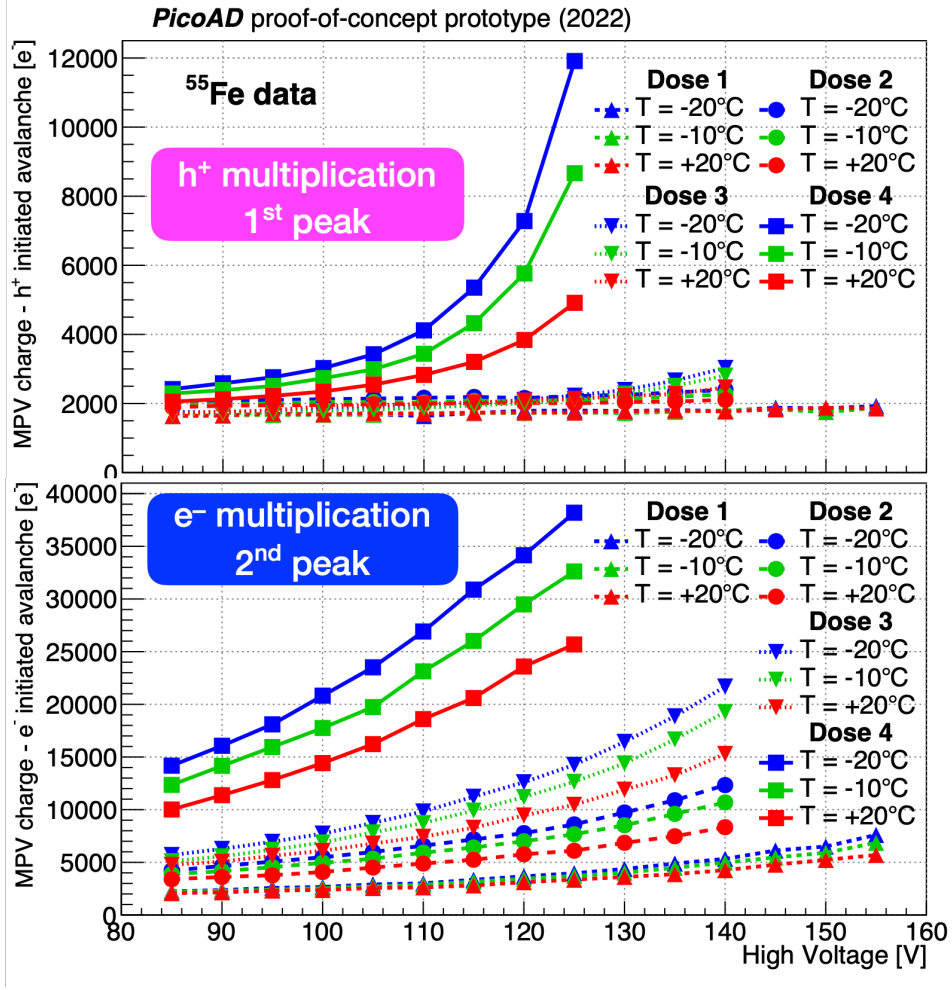
Average amplitudes of h+ and e- gains extracted via gaussian fit around local maxima



Assumption of no gain multiplication when:

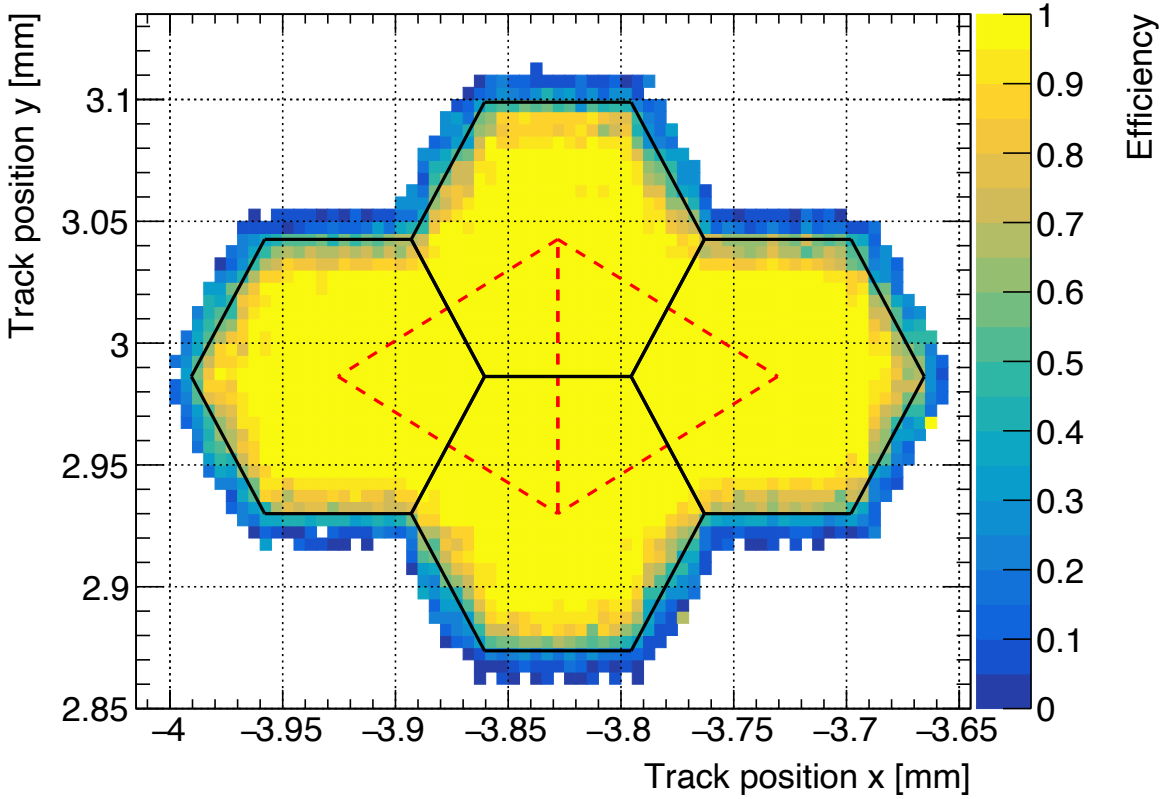
- photon absorbed in drift region
- lowest voltage (85 V)
- lowest dose (dose 1)

normalization value



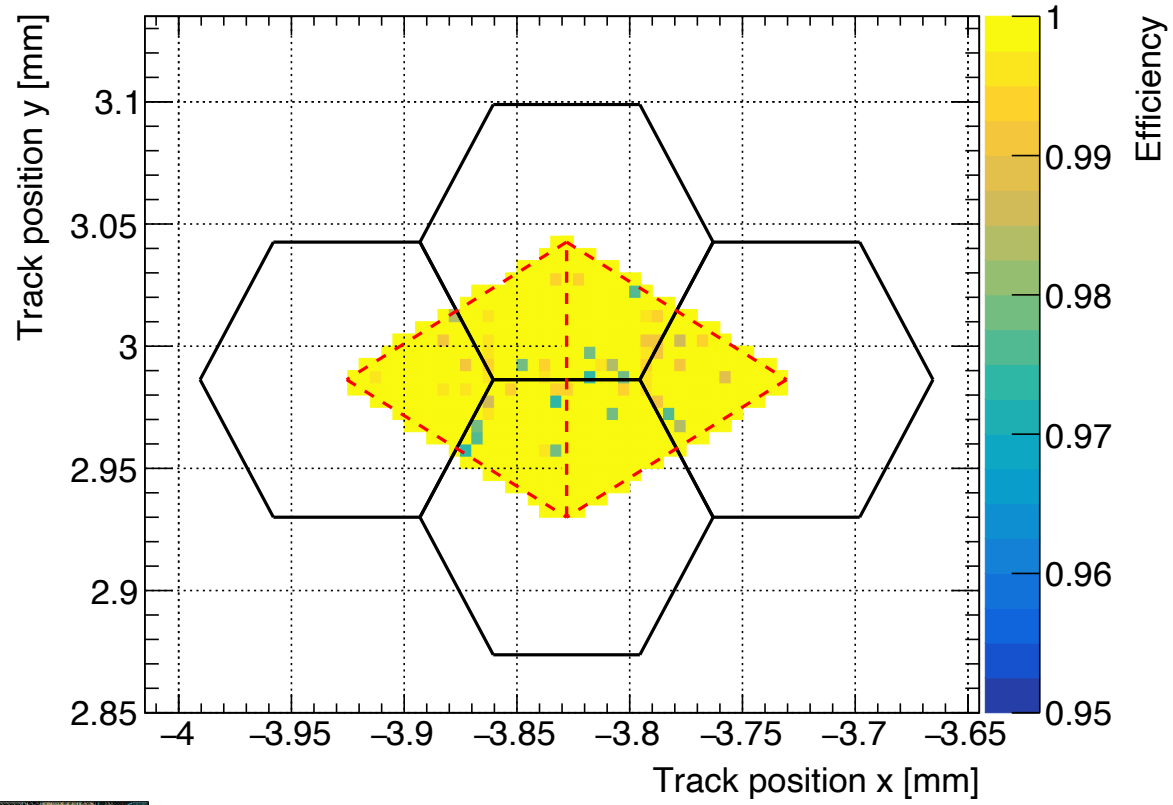
Detection effieciency

PicoAD proof-of-concept prototype (2022)

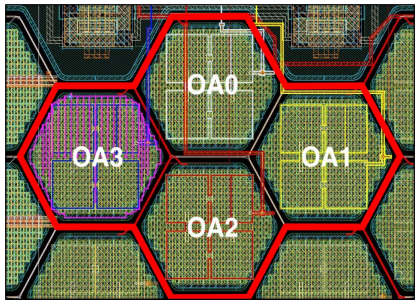


CERN SPS Testbeam: 180 GeV/c pions

V_{th} = 4 mV ; HV = 125 V ; Power = 2.7 W/cm^2



Apparent degradation at the external edges of the four pixels is due to the telescope pointing resolution of ≈10 μm

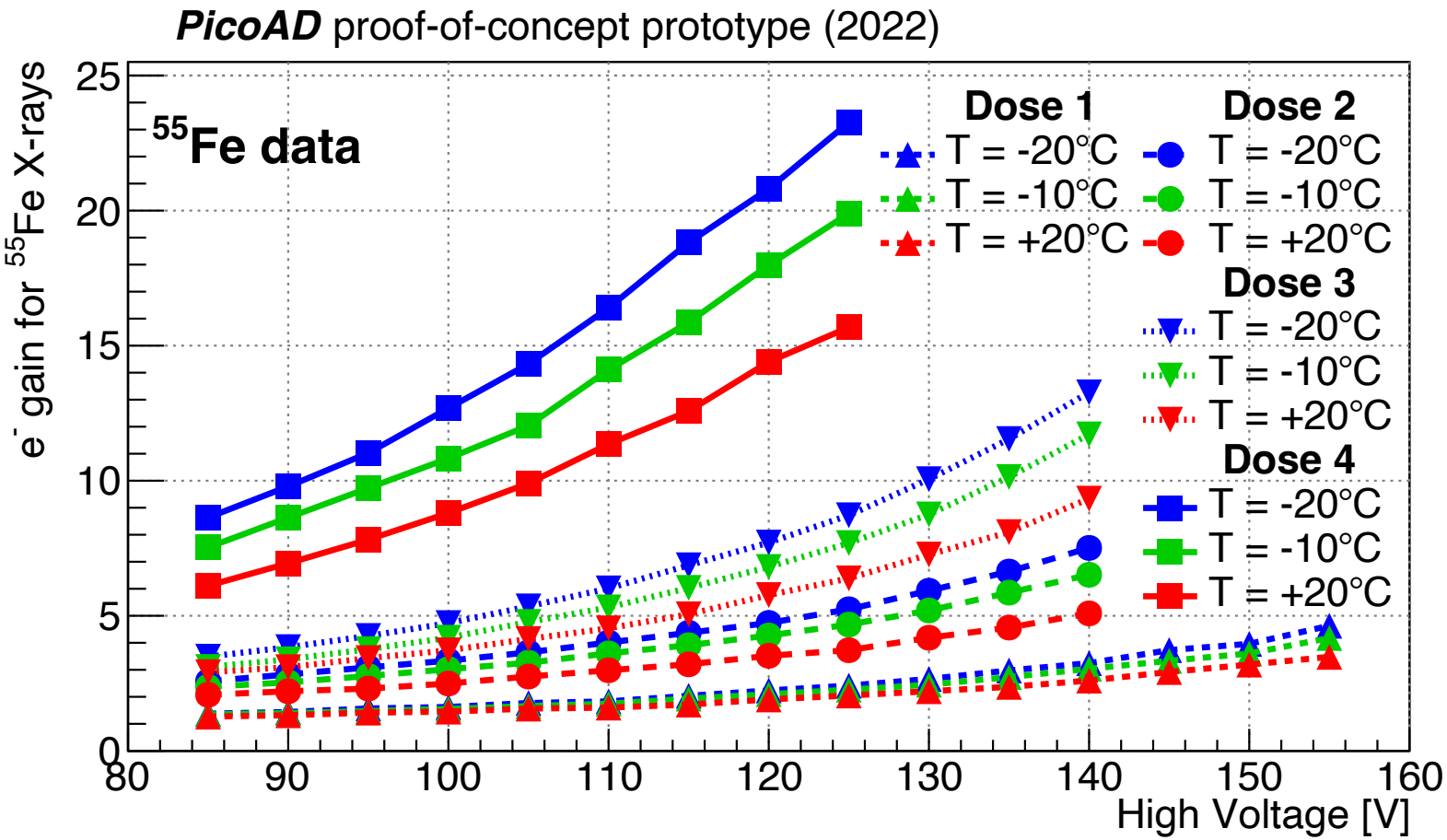


Selection of two **triangles**:

- representative of a whole pixel
- **unbiased** by telescope resolution

Gain measurements I Results

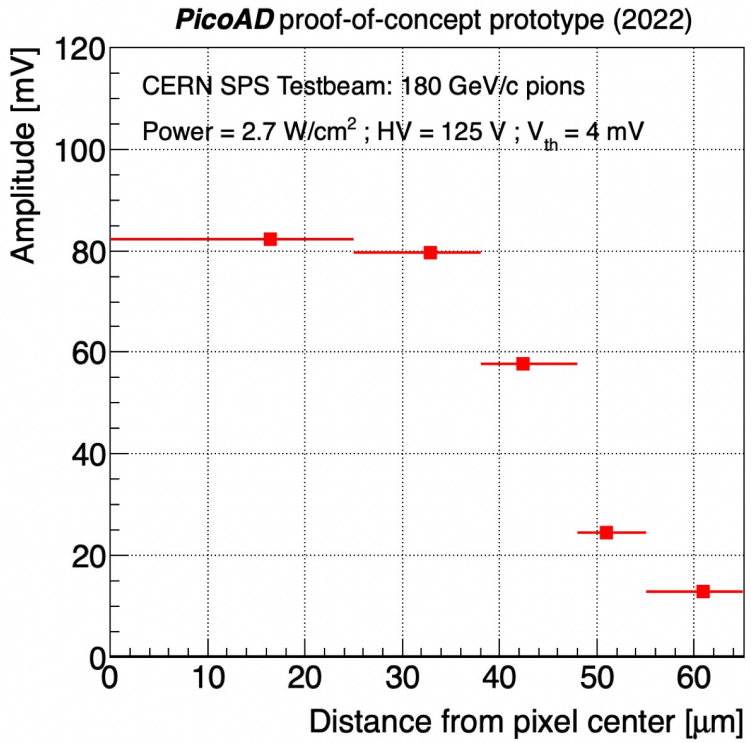
A gain of ≈**20** for ^{55}Fe X-rays is reached at HV = 120 V and T = -20 °C[2]



[2] L. Paolozzi et al., Picosecond Avalanche Detector - working principle and gain measurement with a proof-of-concept prototype. arXiv:2206.07952, June 2022

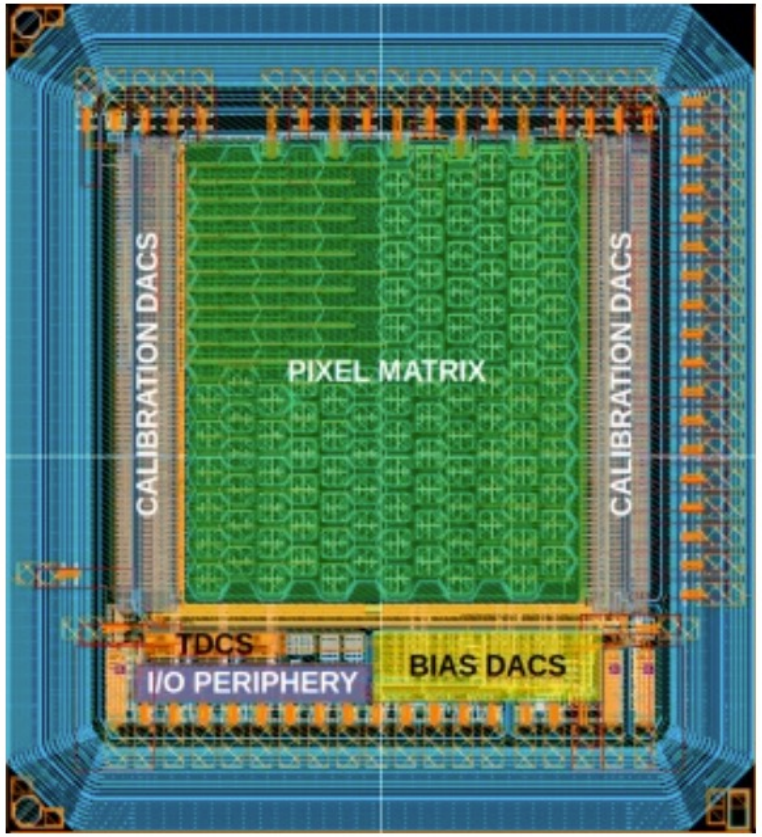
Testbeam results:

Signal amplitude



2019 prototype

100µm pitch hexagonal pixels - 25µm depletion

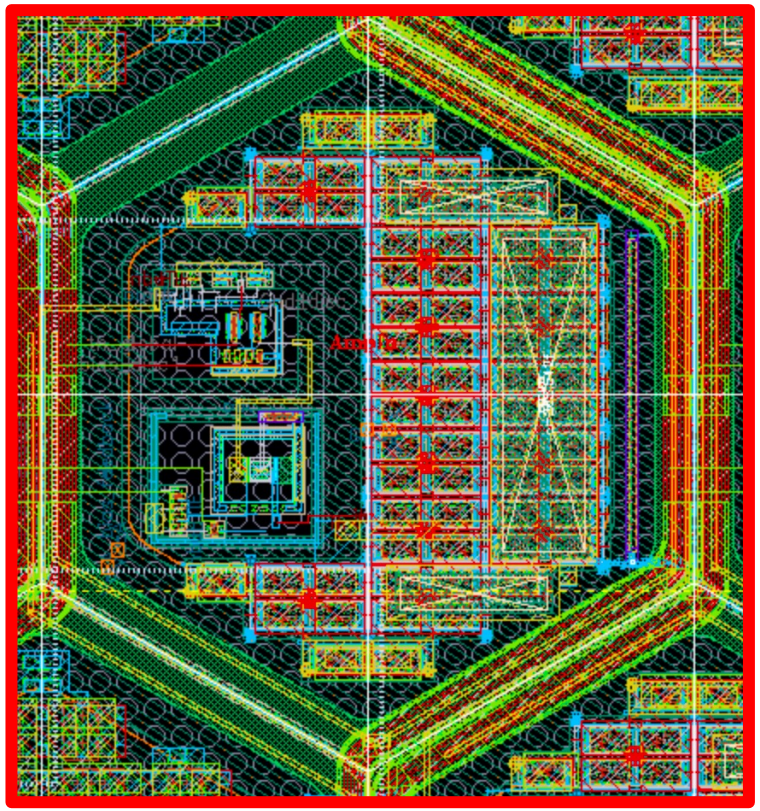


MPW submission in 2019 funded by H2020

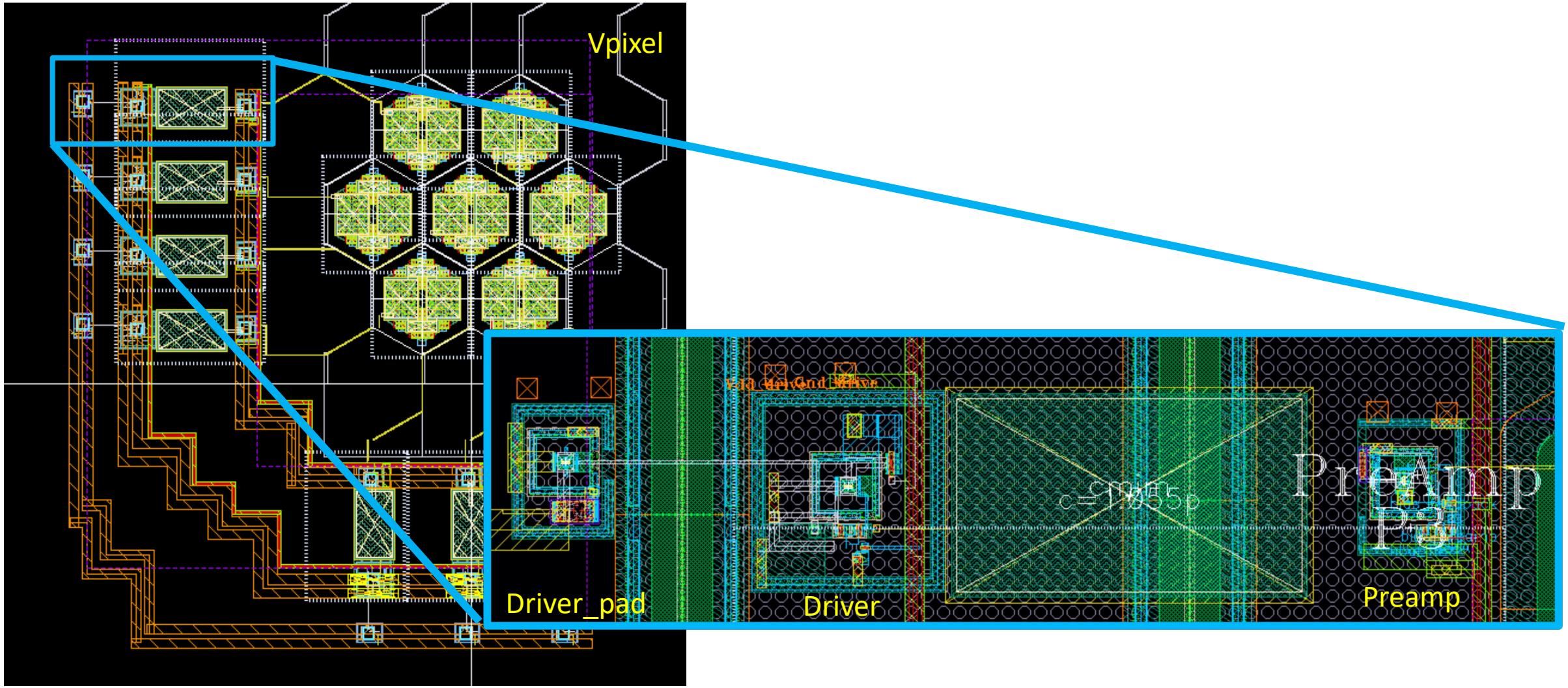
Four Matrices

1. **Active pixel**
   - Front end in pixel
   - HBT preamp + driver (in pixel) + CMOS discriminator (outside pixel)
2. **Active pixel v2**
   - HBT preamp + CMOS discriminator
3. **Limiting amplifier:**
   - HBT preamp + HBT limiting amplifier
4. **Double threshold:**
   - HBT preamp + two CMOS discriminators

Electronic Front-End DM0 I Layout Design



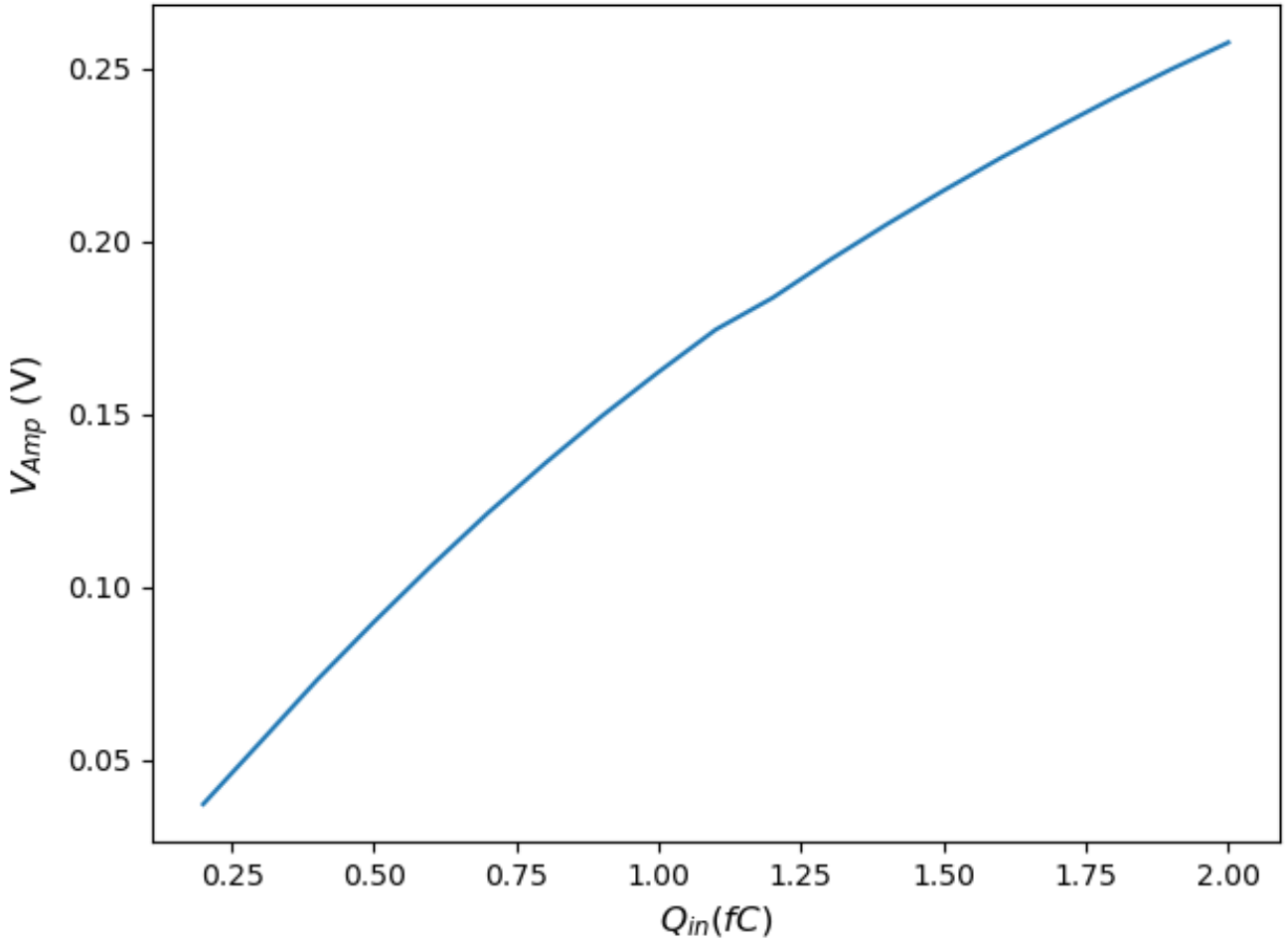
Preamp off-pixel AM1 I Layout Design



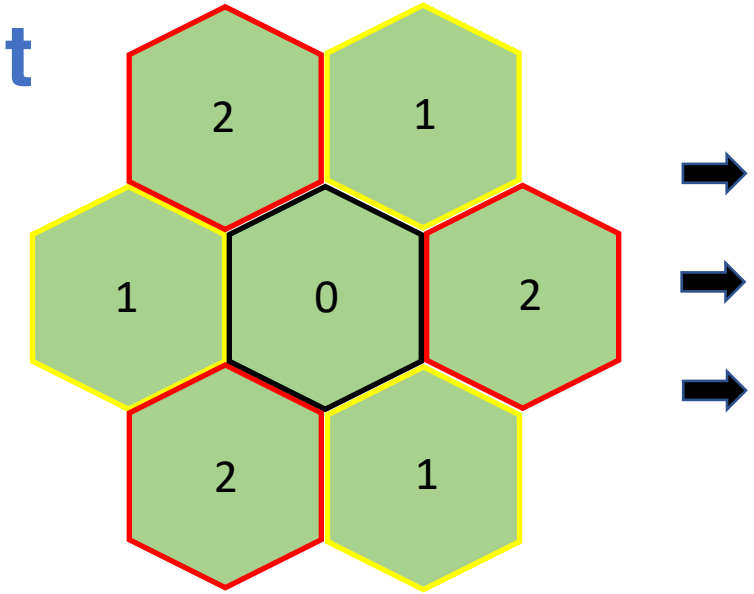
OutPreamp amplitude vs. Input Charge

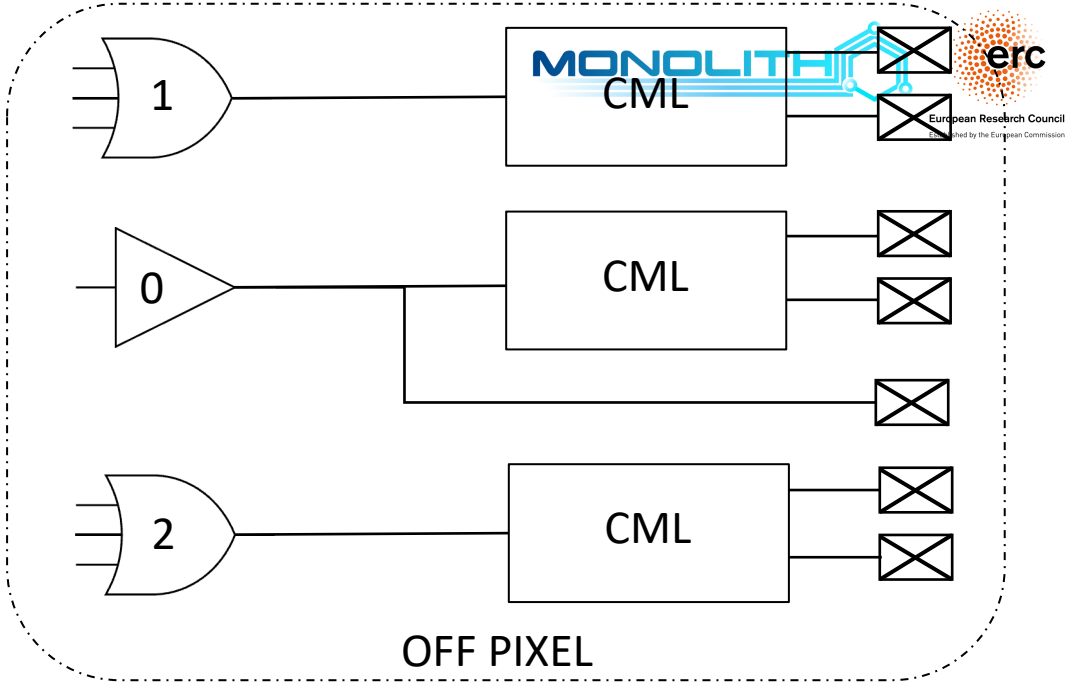
Amplitude of outPreamp signal vs input charge

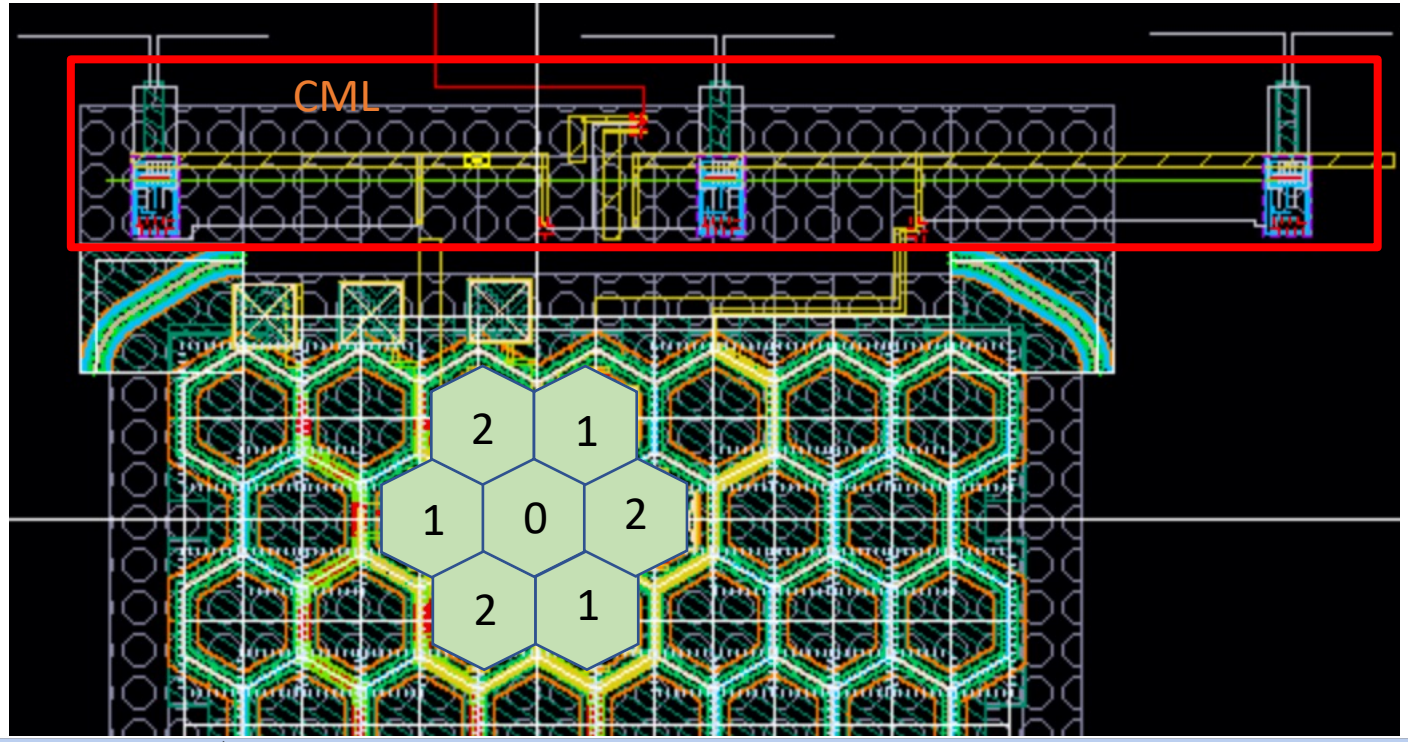
VccA = 1.2 V – Ipreamp= 50 µA – Ifbk= 100nA



CML output







- Group of 3 pixels as input of OR (red and yellow)
- The output are taken differential ended from CML stage
- Pixel0 to study frontend performance