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A Study for a Radiation Tolerant SoC EcoSystem based on Open Source RISC-V hardware for future High Energy Physics applications

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The increase in the complexity and size of modern ASIC designs in the HEP community and the use of advanced semiconductor fabrication processes are strong advocators for employing a System-on-Chip (SoC) design integration methodology. This contribution will present a survey of open-source RISC-V based SoC design platforms and the results of an evaluation study in terms of performance, power and area of three selected RISC-V SoCs. Finally it will propose a Radiation Tolerant SoC interconnect and associated RISC-V core for low performance, low power, fault-tolerant control and monitoring embedded applications.

Summary (500 words)

The increase in the complexity and size of modern ASIC designs in the HEP community and the use of advanced semiconductor fabrication processes are strong advocators for employing a System-on-Chip (SoC) design integration methodology. In a SoC design methodology the designer does not have to develop fully customized RTL code for the target application but instead reuse pre-existing and qualified IP blocks utilizing standardized interconnect busses. Fully customized RTL code requires as much of a design effort as for verification and when design complexity increases so does the verification effort. Developing a set of IP blocks that adhere to standardized interconnect busses enable reusability in multiple designs and applications. These IP blocks are provided verified at the block level and alleviate much of the verification effort at the top level in the target ASIC application. System-on-Chip combines elements of a computer system such as processing cores, memories and peripherals. These elements enable the implementation of re-programmable functions and algorithms thus allowing for flexible and re-configurable embedded hardware. System-on-Chip interconnecting processing elements could enable applications ranging from control and monitoring of on-detector electronics to data processing of physics events.

Within the framework of the EP-R&D WP5 on IC technologies for High Energy Physics (HEP) experiments, we have initiated an activity aiming to propose a System-On-Chip Radiation-Tolerant EcoSystem for use in future ASIC design developments on advanced processes such as a 28nm CMOS technology. We have initiated a survey of open source SoC interconnect platforms. Considering that the RISC-V instruction set is becoming a standard for open-source architectures most of open source SoC platforms are based on RISC-V CPU.

The majority of RISC-V cores are written in higher-level HDLs like Chisel, Bluespec and SpinalHDL, but there are also implementations in SystemVerilog, Verilog and VHDL. Along with the core, usually, full SoC system is provided. The available solutions were surveyed, and three selected candidates were further evaluated in terms of performance, power consumption and area, by performing physical implementation in a 28nm bulk CMOS technology. Several open-source platforms have been studied including the IBEX and Ri5CY cores in the Pulpissimo and Pulpino platforms, Rocket Core in Rocket Chip and PicoRV32 in PicoSoC.

Several interconnect industry standards were evaluated namely AMBA, AVALON, TileLink and Wishbone. Each standard comes with a different level of complexity, ranging from simple non-memory-mapped interconnects like AXI-STREAM (AMBA) to fully cache-coherent and secure interfaces like ACE (AMBA).

Multiple radiation hardening techniques at the RTL level were evaluated for achieving fault tolerance in the SoC. Careful consideration was taken to make the memory system fault-tolerant, applying different strategies

for program and data memory to optimize for area and fault tolerance to Single-Event-Effect compatible with the requirements of detector electronics in hadron colliders.

This contribution will report the results of the open-source SoC platforms, the results of the evaluation study of the shortlisted SoC platforms based on specific RISC-V cores and propose a Radiation Tolerant SoC interconnect and associated RISC-V core for low performance, low power, fault-tolerant control and monitoring embedded applications.

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