Contribution ID: **196** Type: **Oral**

Waveform Sampler: A 2.56GS/s 12-bit Time-Interleaved Pipelined-SAR Analog-to-Digital Converter (ADC) with on-chip Memory

Thursday 22 September 2022 12:00 (20 minutes)

We report the development of a Waveform Sampler (WS) including the design and measurement results. The WS is developed as part of the Endcap Timing Readout Chip (ETROC) for the CMS MTD Endcap Timing Layer (ETL) for the HL-LHC. One of the ETROC 16x16 pixels is equipped with the waveform sampler, to sample the pixel's preamplifier output waveform at 2.56GS/s and convert it into digital domain. This is similar to using an oscilloscope to record the waveform except this is on chip. The reconstructed waveforms will be used for periodically LGAD signal monitoring purposes during the CMS ETL detector operation.

Summary (500 words)

The development of the WS chip consists of three versions. The first version is a 12-bit 320 MS/s single-channel ADC. To achieve such sampling speed and resolution while keeping a relatively low power consumption, we choose Pipeline-SAR architecture as the pipeline structure improves the overall conversion speed and alleviates the noise and linearity requirement for the LSBs. In addition, the SAR architecture is mostly digital, which benefits from technology scaling and has high power-efficiency. The single-channel ADC consists of a 6-bit SAR as the first stage, a dynamic residue amplifier and a 7-bit SAR (with 1-bit interstage redundancy) as the second stage. Implemented with 65nm CMOS technology process, the single-channel ADC can operate up to 350MS/s and achieve an Effective-Number-of-Bits (ENOB) of 9.6 Bits at Nyquist input frequency (˜170 MHz). The measured power consumption at 350 MS/s is 2.86 mW.

The second version of the WS chip consists of an 8-channel Time-Interleaved ADC and an on-chip memory. By interleaving 8 single-channel sub-ADCs, each operating at 320 MS/s, the 8-channel ADC achieves a total sampling rate of 2.56 GS/s. In addition to the eight sub-ADCs, the WS consists of a clock generation block that generates the eight interleaved non-overlapping sampling clocks for eight sub-ADCs, and a distribution network that delivers the clocks and input signals to eight sub-ADCs. A dedicated Y-tree network is implemented to minimize the time skew of the clocks as well as the distortions on the inputs caused by the coupling capacitance. At 2.56 GS/s, the WS achieves an ENOB of 9.0 Bits at the Nyquist input (˜1.2 GHz). The on-chip memory consists of eight sub-memory blocks that write at 320 MHz in parallel. Each sub-memory stores the digital output from one sub-ADC and has depth of 1024. Overall, the on-chip memory can store the digital outputs of 8192 samples from the 2.56 GS/s ADC. The readout data from the memory can be used to reconstruct the LGAD signals in a 3.2 ⊠s time window.

The third version of the WS chip is the rad-hard version that will be integrated inside the ETROC2 chip. An amplifier with high linearity has been implemented in the WS chip to provide some extra gain, so that the ADC can still monitor the LGAD signal from the preamplifier when the LGAD gain is reduced towards the end of HL-LHC operation. The amplifier can be bypassed to monitor the preamplifier signal directly. The depth of the on-chip memory has been modified to 1024, corresponds to a 400 ns time window (16 bunch crossings), to save the area. We adapted the latch-based memory provided by CERN ASIC Support Team for the on-chip memory for this version to save the power consumption. Overall, the power consumption of WS is 117 mW when enabled momentarily for monitoring purpose, of which 12 mW is consumed by the memory. This prototype has been tested with the ETROC0 preamplifier. The reconstructed WS output shows good agreement with the preamplifier output, which verifies the functionality of the amplifier and ADC.

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Session Classification: ASIC

Track Classification: ASIC