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The Design and Testing of the COLDATA Concentrator ASIC for the Deep Underground Neutrino Experiment

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COLDATA is the data concentrator ASIC for the Liquid Argon Time Projection Chamber (LArTPC) Far Detector of the Deep Underground Neutrino Experiment (DUNE). This ASIC will operate for its lifetime at cryogenic temperatures immersed in LAr. Two COLDATA, eight ColdADC, and eight LArASIC front-end ASICs are placed on each Front-End Motherboard (FEMB) in the LArTPC. Each COLDATA concentrates the data output from four ColdADC ASICs (64 front-end channels) onto two 1.25 GHz serial lines. The COLDATA also provides clock generation and control, slow and fast command response, and reset control for the Front-End Motherboard.

Summary (500 words)

The Deep Underground Neutrino Experiment (DUNE) [1] Far Detector uses Front-End Motherboards (FEMBs) throughout its Liquid Argon time projection chamber (LArTPC). Each FEMB (see Figure 1) sits inside the cryostat immersed in Liquid Argon, services 128 TPC channels and communicates to a Warm Interface Board (WIB) outside of the cryostat. Each FEMB houses eight LArASIC front end ASICs [2] to amplify and shape TPC outputs, eight ColdADC ASICs to convert the LArASIC outputs to digital signals, and two COLDATA ASICs. COLDATA_E4 is the fourth and final COLDATA and is the production version that will be used by DUNE. This presentation is the first public discussion of the COLDATA design and methodology. Reference [4] showed cryogenic test results for a few sub-circuits, but did not discuss the overall design.

COLDATA is the data concentrator chip for data from the TPC. Furthermore, all inbound communication either passes through one or both COLDATA ASICs or is acted upon by one or both COLDATAs. Inbound data includes clocks, fast (encoded, time-sensitive) commands, and slow control commands. The slow control interface uses an I2C-like [5] protocol.

For the following paragraphs see Figure 2.

On the FEMB, both COLDATA and all ColdADC chips are individually addressable by I2C. Since I2C requires responses, one COLDATA (COLDATA_TOP) receives the communication from the WIB and relays it to the other COLDATA (COLDATA_BOT). Each COLDATA then relays the I2C command to their respective ColdADCs. Responses are routed back appropriately. I2C registers are distributed throughout the COLDATA chips, and intra-chip communication is handled using a classic wishbone-like bus system.

The LArASIC chips all use a custom SPI-like interface. The COLDATAs maintain internal registers containing LArASIC configuration information and, when required, communicate those values to the front-end chips.

COLDATA receives a 62.5 MHz clock from the WIB. It relays that clock to each of its ColdADC chips and it creates a 2 MHz ADC sample clock using simple digital processing. The edges of the 2 MHz clock are adjustable through fast command to allow system-wide synchronization of the sample periods. Despite the simplicity of the digital processing, these clocks show low jitter.

Fast Command permits action on time-sensitive issues like reset, time-stamp synchronization, and 2MHz clock edge control.

Since the COLDATA are in a cryostat many meters from the WIB, a dedicated reset signal is impractical. Instead, COLDATA has a power-on reset and a fast command-based reset. Both trigger a simple state machine

that resets and enables different parts of the chip at the proper time.
COLDATA captures the individual data frames from four ColdADCs, packs them into one of several user-chosen frames, encodes the frames by 8B10B, and passes the encoded data to a serializer.
The COLDATA PLL is capable of functioning at both warm and cold. It receives the same 62.5 MHz clock used by the Clock Generation and Relay modules, creates a 1.25 GHz output clock, and serializes the data output by the Data Processing modules. The PLL and serializer performance can be optimized through slow control.

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