RAFAEL : A Clock and Data Fan-Out ASIC for CMS HL-LHC Upgrades

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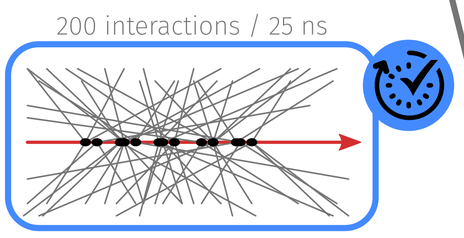
Timing in HL-LHC

In order to achieve tens-of-ps particles time-tagging performance required at HL-LHC, the CMS clock tree is being upgraded

☆ Particle time tagging ≈ 35 ps

➜ **Clock distribution with a jitter < 15 ps RMS**



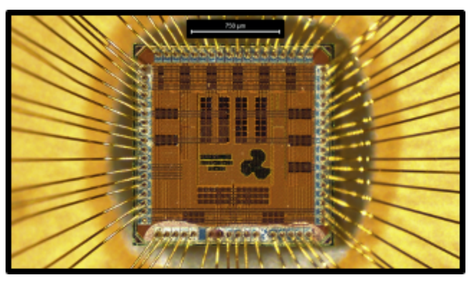


Photo of RAFAEL in an open cavity package

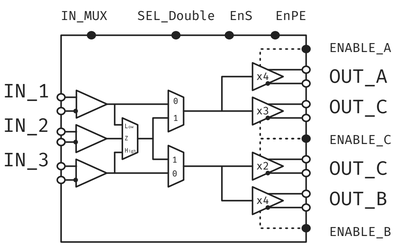
A radiation-hard fan-out ASIC, named RAFAEL, was developed in a 130 nm CMOS technology to **distribute the clock and the data** to the frontend ASICs of the CMS detectors that require precision timing

RAFAEL main characteristics

☆ Simple ASIC : No slow control, no clock resync. ➜ easy to use.

☆ CLPS inputs - outputs ➜ compatible with phase II Front End

- **3 inputs** ➜ Internal Mux ➜ Up to **13 outputs**.
- Outputs divided in 3 banks (A, B, C) to adjust the power consumption
- Output signal strength and pre-emphasis external settings



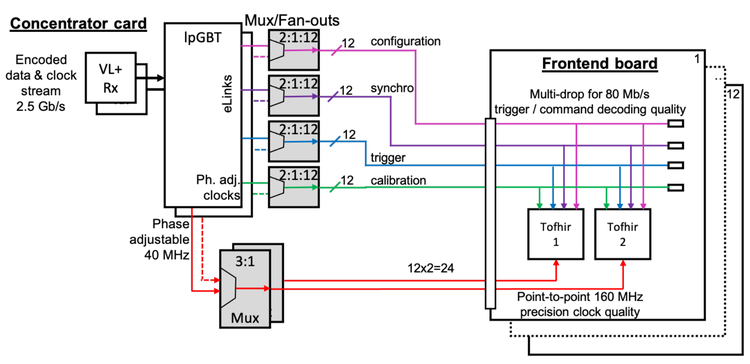
☆ Low additive **jitter < 4 ps** for $f_{input\_signal} \in [40 : 320]$ MHz

☆ Standard JEDEC QFN 48 package

	Sim	Meas.
Idle	9 mA	7.2 mA
Fin = 40 MHz	39 mA	38.1 mA
Fin = 400 MHz	110 mA	111.8 mA

CMS Use Cases

BTL use case : Mux fanout buffer



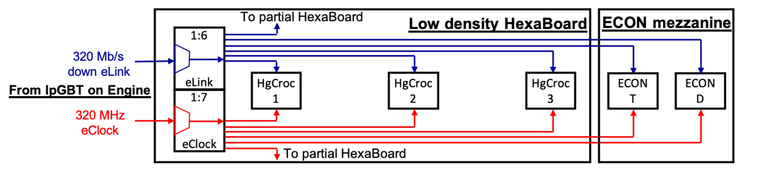
For BTL, up to 6 RAFAELs are foreseen on the Concentrator Card (CC). 12 outputs are used per ASIC.

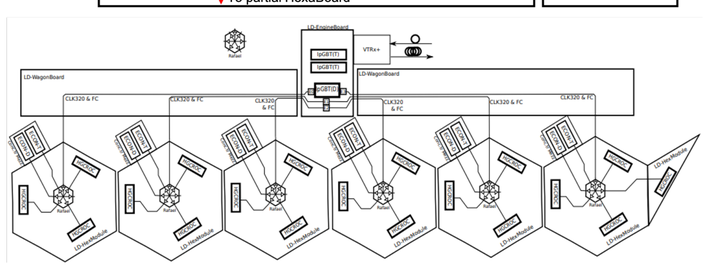
BTL benefits from RAFAEL input mux capability to add **system redundancies** : the CC board is resilient to a communication failure with the DAQ

☆ About 3000 RAFAELs

☆ Main challenges : Signal integrity & power consumption

HGCAL use case : double fanout buffer





For HGCAL, RAFAEL is used to distribute simultaneously the clock and the fast command to the Front End ASIC : HGCROC

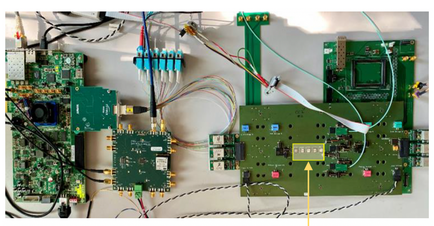
HGCAL benefits from the build-in double buffer mode to use RAFAEL as **two independent fanouts**

☆ About 36 000 RAFAELs

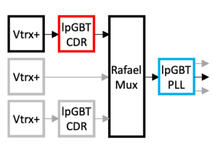
☆ Main challenges : Signal cross-talk & radiation hardness

RAFAEL-V0 (2019) — BTL ✓

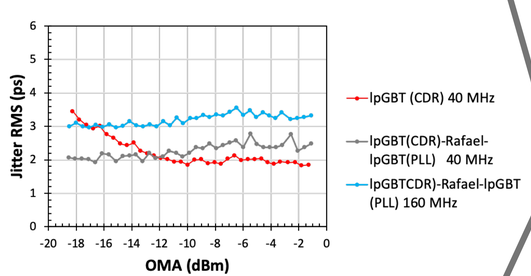
BTL clock distribution intensive tests



Signal integrity test using CCv2



Schematic diagram of the testbench with LpGBT V0

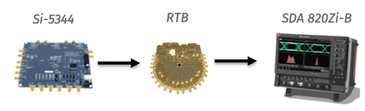


Clock Jitter of RAFAEL + LpGBT V0 vs optical power

☆ RAFAEL **validated in single buffer mode**

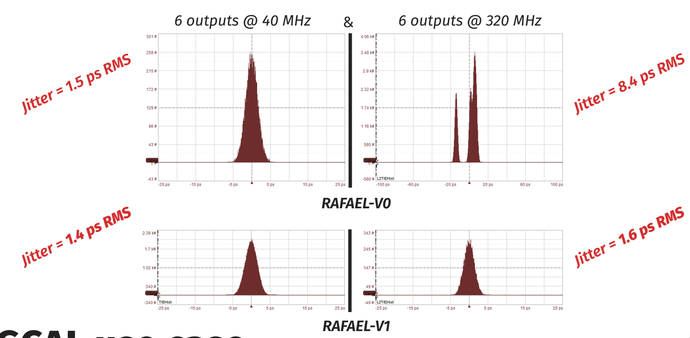
RAFAEL-V1 (2020) — HGCAL ✓

Signal cross-talk in double buffer mode



RAFAEL V0 with half of the ASIC driving a 40 MHz clock to 6 outputs and the other half driving a 320 MHz clock to 6 outputs

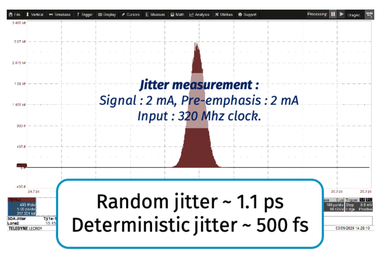
➜ RAFAEL V1 in the same conditions with improved on-chip power distribution network



☆ RAFAEL **validated for HGCAL use case**

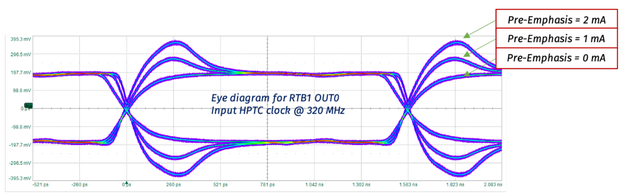
Highlight of RAFAEL performance study

✓



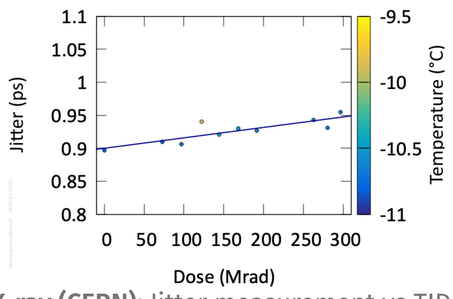
In-Lab : Jitter measurement with an HPTC board providing the 320 MHz input clock and an high end oscilloscope

✓



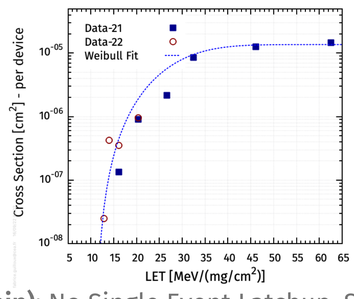
In-Lab : Output signal amplitude, additional pre-emphasis & pre-emphasis duration could be externally set to adjust to the driven lines impedance

✓



X-ray (CERN): Jitter measurement vs TID. No degradation observed

?



HIF (Louvain): No Single Event Latchup. Single Event Transient to be measured with protons at ARRONAX

Qualification test bench

☆ Robot available @ IRFU (production qualification foreseen in the industry)

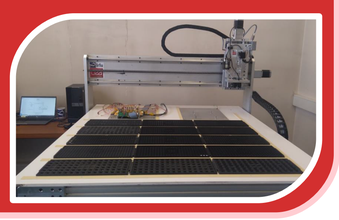
➜ Anticipate final production DAQ development

➜ Statistic and final acceptance criteria

☆ Python DAQ + SAMPIC system :

➜ 32 channels with time resolution ≈ 5 ps RMS/ch

➜ Full characterization in 30 secondes



Conclusion

☆ RAFAEL fulfills BTL & HGCAL requirements

☆ Full characterisation in lab, with TID, NIEL and Ions

➜ SET seen with ions ➜ Not representative of the LHC environment ➜ proton tests in Sept. 22

➜ Characterization system for mass production qualification test ready

RAFAEL PRR & ASIC production : end of 2022