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RAFAEL : A Clock and Data Fan-Out ASIC for CMS HL-LHC Upgrades

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In order to achieve tens-of-ps particles time-tagging performance required at HL-LHC, the CMS clock tree is being upgraded. A radiation-hard fan-out ASIC, named RAFAEL, was developed to distribute the clock and the data to the frontend ASICs of the CMS detectors that require precision timing, including BTL and HGCAL. Its main constraint is a low additive jitter, less than 4 ps RMS, even after 300 Mrad and $5 \cdot 10^{16}$ n_{eq} 1 MeV/cm^2 irradiation. The chip architecture is presented along with its performance in the substantially different use cases proper for BTL and HGCAL.

Summary (500 words)

Timing precision of ˜35 ps required for the particle detection at HL-LHC can only be achieved with a system clock distribution tree ensuring the synchronization of electronics channels at less than 15 ps RMS level. The last stage of this tree within the frontend boards of the CMS BTL and HGCAL detectors, is formed by the lpGBT and subsystem-specific frontend ASICs. To facilitate the distribution of the clock and the downstream data from lpGBT to the ASICs, a radiation-hard fan-out chip named RAFAEL was developed.

The flexible architecture of the fan-out allows satisfying the two substantially different requirements of the BTL and HGCAL frontend designs. In the BTL use case, the ASIC is configured as a single large fan-out to deliver either clock or data signals to up to 12 pairs of fronted ASICs. The fan-out offers the possibility to choose the signal source between its two inputs, thus ensuring the clock/data distribution redundancy within the BTL frontends. In the HGCAL use case, the ASIC is configured as two smaller independent fan-outs delivering simultaneously the clock and the data on its inputs to up to six fronted ASICs.

RAFAEL has 3 inputs and 13 outputs, supporting a wide range of differential signal interfaces including the CERN low voltage signaling, offered by lpGBT. External configuration pins allow to choose between the two configurations, to set the output signal parameters, such as driving strength, pre-emphasis and its duration, and to deactivate groups of outputs for power saving. The architecture of the ASIC is kept simple, without internal memory nor internal signal sampling, in order to handle the harshest radiation environment of the detector frontends.

The ASIC was thoroughly tested in laboratory to validate its low additive jitter of less than 4 ps within the clock range of interest from 40 MHz to 320 MHz, at various temperature, power supply or input signal strength. A special care has been paid to the design of the power distribution network in order to minimize the crosstalk between the two half-buffers, ensuring minimal influence of the data activity in the chip on its clock distribution performance. Intensive radiation test campaigns were performed for TID, NIEL and SEE, showing that the ASIC complies with the most demanding requirements of both sub-systems.

In addition to laboratory tests, a specific test-stand for the mass production of the ASIC has been designed. Based on a board with a test socket, coupled to the SAMPIC 8.6 GSPS sampling data acquisition system, the production test bench was successfully interfaced with an automatic pick and place robot. Controlled by a python-based software, the test stand is able to classify the production ASICs in about 30 sec, measuring, among other relevant parameters, the clock jitter on all of its 13 differential outputs with an accuracy of about 5 ps. Tens of RAFAELs are currently successfully used within the sub-detector frontend board prototypes. About 45 000 units will be produced by early 2024 to satisfy overall CMS needs.

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