



Contribution ID: 71

Type: Poster

Characterisation of the first digital modules with RD53B-CMS readout chips for the Phase-2 Upgrade of the CMS Inner Tracker

Thursday, 22 September 2022 16:40 (20 minutes)

To cope with the challenges posed by the High-Luminosity LHC, the CMS experiment will feature a new silicon tracker. The modules for the inner tracker are hybrid silicon pixel modules based on a new readout ASIC, developed by the RD53 Collaboration, capable of sustaining higher hit rates and radiation levels and enabling the use of serial-powering chains. The qualification of the latest version of the RD53 chips (RD53B) is underway, and it will lead to the final version of the readout ASIC for CMS. This contribution will present results of tests on the first digital modules featuring the RD53B-CMS chip.

Summary (500 words)

The High-Luminosity phase of the LHC will bring new challenges to its experiments.

The CMS experiment will have to cope with an instantaneous luminosity of up to $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ (corresponding to up to 200 pileup collisions per bunch crossing), and collect data for an integrated luminosity of up to 4000 fb^{-1} , approximately ten times the amount of data to be recorded before the HL-LHC. In addition, detector data will be read out at up to 750kHz (to be compared to the current 100kHz), and the trigger latency will be increased from the current 3.2 μs to 12.5 μs .

To cope with these conditions, CMS will use a new and improved silicon tracker. The innermost part of this system, or Inner Tracker, will be comprised of 3892 hybrid modules featuring pixel sensors bump-bonded to a new readout ASIC. The new sensors are characterised by higher granularity ($2500 \mu\text{m}^2$ in pixel size) and reduced thickness (150 μm) compared to the current pixel detector, to maintain and possibly improve tracking performance under the higher levels of pileup and irradiation of the HL-LHC. The new readout ASIC, developed by the RD53 Collaboration using 65nm CMOS technology, is designed to cope with hit rates up to 3-4 GHz/ cm^2 for trigger latencies up to 12.5 μs and radiation levels of up to 500 Mrad, with an in-time pixel threshold as low as 900 electrons. The readout chip also features Shunt-LDO regulators to enable the operation of multiple pixel modules (up to 12) in serial-powering chains, an innovative design choice aimed at minimising the material budget of the detector.

The first version of the RD53 readout chip (RD53A) was used to make the final design choices for the ASICs to be used for ATLAS and CMS trackers, and it was tested extensively to qualify all the functionalities of the readout chip, including tests with modules and system prototypes. The production of the next generation of RD53 chips (RD53B) has started over the course of the last year, and its qualification will define the final version of the chip to be used by the experiments.

First digital modules featuring the RD53B-CMS chip have been assembled in early 2022 as part of the development of the Tracker Endcap Pixel (TEPX) subdetector of the CMS Inner Tracker. This contribution will present the results of tests done on these first RD53B-CMS digital modules.

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Session Classification: Thursday posters session

Track Classification: ASIC