An SEU occurs in a block without majority voter feedback. The stored data is not altered, therefore the discrepancy signal remains permanently active.

A dedicated output pad allows access to the discrepancy signals of the majority voter. For SEUs on the external memory, the discrepancy signal remains active for one clock cycle, and the correction is completed.

The triplicated clock, reset and JTAG signals are available on three dedicated pads. The STRV-R1 contains three separate Power domains to allow finer analysis of the power consumption.

Power Consumption: The system power consumption varies between 29μW and 332μW depending on type of instructions executed. The SRAM refresh algorithm requires an additional 103μW. The measured total leakage power of the unirradiated chip is 110 μW.

Instruction Scenarios: The SRAM centered scenario contains primarily load or store instructions, whereas the register centered scenario only stores data in the general purpose registers. The table shows the power consumption for each domain of the chip at a system clock frequency of 50MHz and a temperature of 25°C.

Performance: Running the Dhrystone 2.1 benchmark the system achieves 0.628 DMIPS/MHz. Using the O3 GCC compiler option yields a value of 0.665 DMIPS/MHz.