STRV – A radiation hard RISC-V microprocessor

TWEPP 2022 Topical Workshop on Electronics for Particle Physics

Currently microprocessors are precluded from the use in several high-energy physics applications due to the harsh radiation present. The STRV-R1 (SEU-tolerant-RISC-V) microprocessor aims to overcome this limitation and replace the custom digital control logic found in current ASICs. A triple modular redundancy (TMR) based protection scheme is applied to protect the RISC-V microprocessor core against radiation induced soft errors. The implementation has been done in a 65nm CMOS technology.

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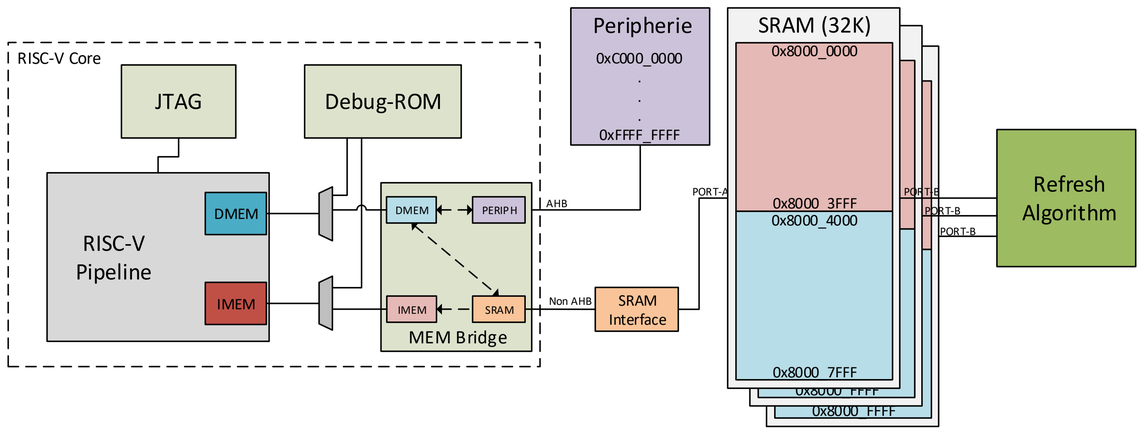
System Architecture

RISC-V RV32-IMC Core

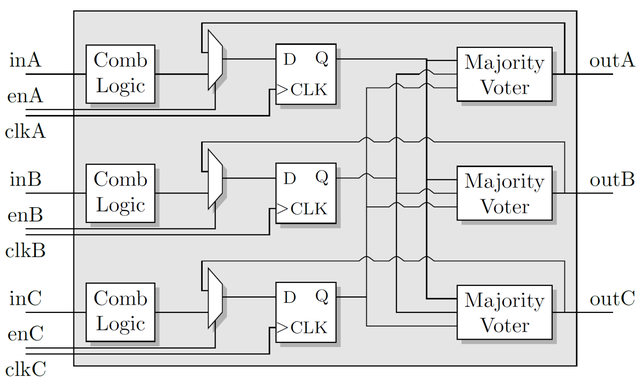
- Based on AIRISC Core from Fraunhofer IMS
- 3 stage pipeline (fetch, decode/execute, writeback)
- Multiplication extensions
- Compressed instruction extension

Debug Module: The integrated Debug Modul with its accompanying debug ROM allows debugging of the core and programming of the SRAM via a JTAG TAP

Memory Layout: Instructions and data are stored within the same 32kB SRAM. This enables a flexible layout with an adjustable ratio between program and data memory size. During the execution phase of a load or store instruction the IMEM bus access to the SRAM is blocked and the pipeline is stalled.
The use of dual-port RAM allows a self-refresh of the memory content independent of the core.



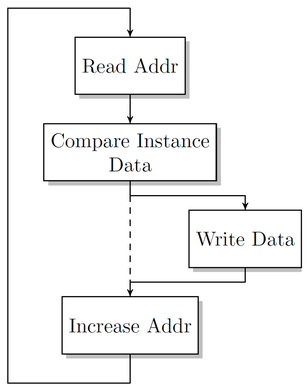
SEU Protection Schema



Triple Modular Redundancy: The main goal of using triple modular redundancy throughout the design is to eliminate all single points of failure. STRV-R1 uses full TMR, meaning a triplication of all combinational logic, all sequential logic elements, and the use of three separate clock trees for the sequential logic. STRV-R1 contains a voter after every sequential element (fine grained TMR) ensuring that the following combinational logic is not exposed to erroneous signals.

Storage Elements: To prevent the accumulation of errors in sequential elements that are not updated every clock cycle, they must be refreshed. A feedback path is added, that updates sequential elements with the majority voted content via a multiplexer, when no new data is to be stored. The feedback guarantees that a SEU in a sequential element is corrected within the next clock cycle.

SRAM: Three SRAM blocks in a TMR configuration are used as the main instruction and data memory in the STRV-R1. Accumulations of SEUs in the SRAM is a major concern, since there is no upper time limit between write accesses. STRV-R1 relies on a self-refresh algorithm that refreshes the SRAM content with corrected data. This scrubbing algorithm is fully independent from the RISC-V core. The system uses dual-port SRAMs to provide the RISC-V core and the self-refresh algorithm with independent access to SRAM content. The scrubbing algorithm can refresh the complete memory within 164µs – 328µs.



Monitoring: The majority voters have an output signal that indicates the detection of an discrepancy. The discrepancy signals are forwarded to a counter via an or-gate tree. This allows the counter to track the number of SEUs occurred within the domain. The value of the counter can be accessed from the RISC-V core.

STRV-R1 Implementation

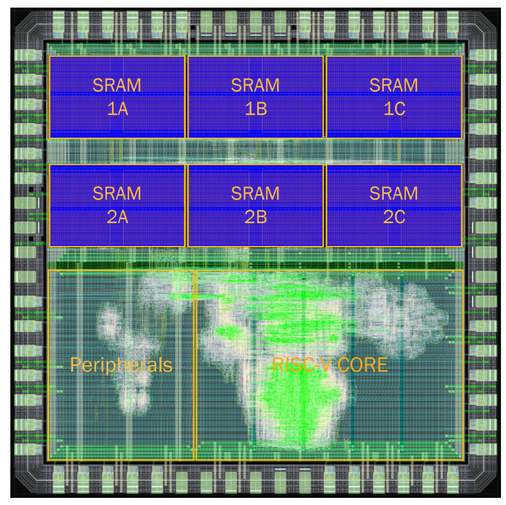
Key Facts:

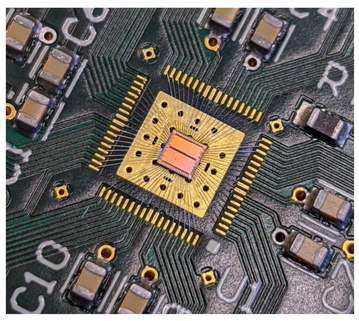
65nm CMOS Technology
2mm x 2mm Die size
1.2V Supply Voltage
50MHz System Clock Frequency
3x32 Kbyte Dual-Port SRAM

Interfaces:

16550 compatible UART, JTAG, 27 GPIOs
External Interrupt

The 32bit wide Dual-Port SRAM is made up of two 16bit wide macros with the SRAM Interface placed in-between. The redundant instances of each TMR group are spaced at least 15µm in an imbricated pattern to prevent multiple upsets in the same group. The triplicated clock, reset and JTAG signals are available on three dedicated pads. The STRV-R1 contains three separate Power domains to allow finer analysis of the power consumption.





Parameter	Non-TMR	TMR Design	Ratio
Core gate count[a]	17.2k	88.5k	5.14
Total system sequential gates[a]	3.3k	11.1k	3.29
Total system gate count[a]	19.6k	109.9k	5.60
Total system cell count[b]	27.1k	138.7k	5.12
Total majority voter count	-	11.3k	3.24
SRAM area requirement	0.38mm²	1.23mm²	4.96

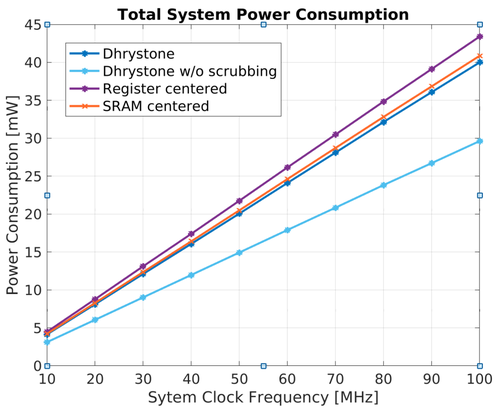
[a]Gate count after synthesis [b]Cell count of the final ASIC design

Power Consumption

Power Consumption: The system power consumption varies between 298µW/MHz and 332µW/MHz depending on type of instructions executed. The SRAM refresh algorithm requires an additional 103µW/MHz. The measured total leakage power of the unirradiated chip is 110 µW.

Instruction Scenarios: The SRAM centered scenario contains primarily load or store instructions, whereas the register centered scenario only stores data in the general-purpose registers. The table shows the power consumption for each domain of the chip at a system clock frequency of 50Mhz and a temperature of 25°C.

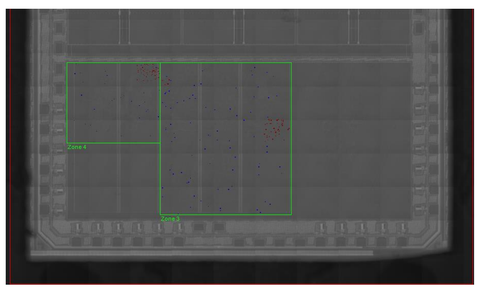
Scenario	Power Consumption [mW] Core	SRAM	Peripherals	Total
Dhrystone Benchmark[a]	7.33	10.26	2.49	20.08
Register centered[b]	8.55	10.68	2.55	21.77
SRAM centered[c]	7.61	10.44	2.45	20.51
[a] w/o SRAM refresh	7.33	5.12	2.49	14.94
[b] w/o SRAM refresh	8.54	5.54	2.55	16.63
[c] w/o SRAM refresh	7.61	5.30	2.46	15.37



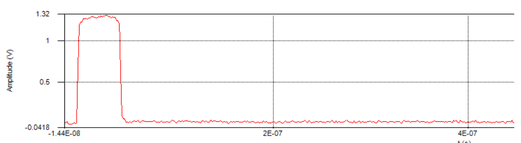
Performance: Running the Dhrystone 2.1 benchmark the system achieves 0.628 DMIPS/MHz. Using the O3 GCC compiler option yields a value of 0.665 DMIPS/MHz

SEU Laser Tests

Single Event Effects: The SEU tolerance of the STRV-R1 was verified by introducing SEUs using SPA backside-illumination. The triple modular redundancy and majority voter placement scheme introduced in the STRV-R1 design have proven effective. Occurring SEUs are immediately detected and corrected within one clock cycle by the integrated feedback. The triplication of SRAM content and the accompanying scrubbing algorithm provide reliable correction of disturbed data and instructions.

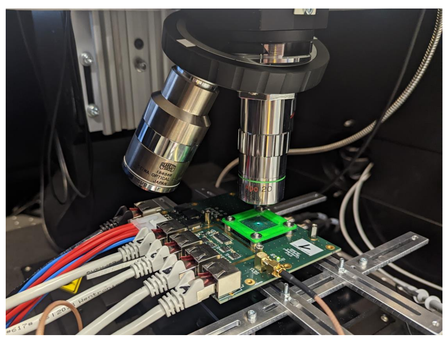


Mapping: Function blocks with triplication and majority voters but without a mechanism for immediate correction of SEUs can be easily identified in a superimposed map of the chip. They are marked as red dots.



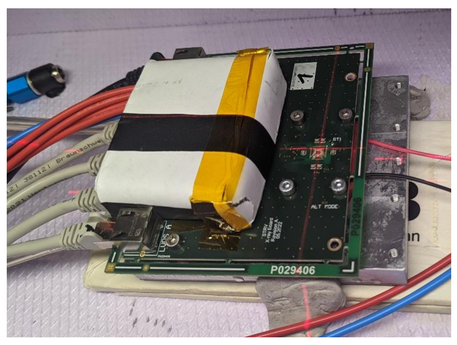
A dedicated output pad allows access to the discrepancy signals of the majority selector. An SEU is detected and corrected. The discrepancy signal remains active for one clock cycle until the correction is completed.

An SEU occurs in a block without majority voter feedback. The stored data is not updated, therefore the discrepancy signal remains permanently active.



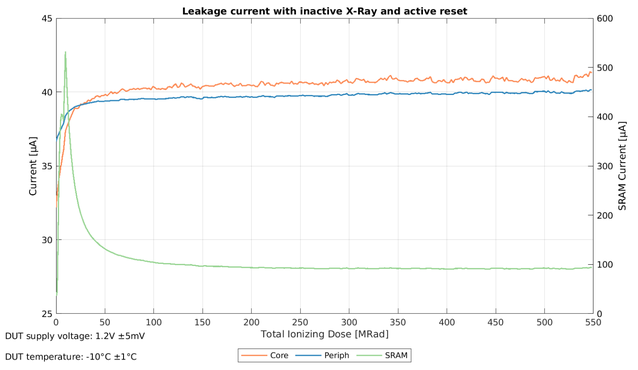
X-ray Irradiation

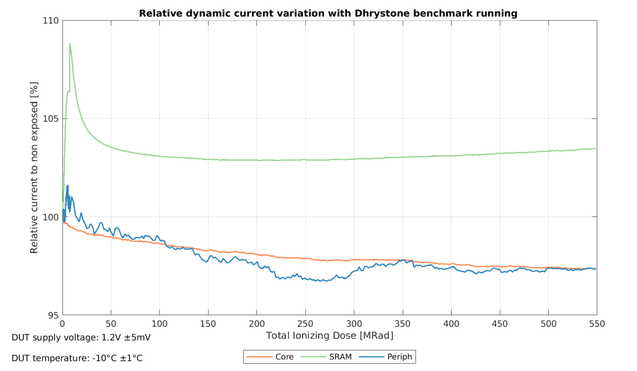
TID effects: TID effects are targeted through the use of a 65nm fabrication technology in combination with thin gate oxide transistors which achieves an inherently high TID hardness. The exclusive use of thin gate oxide transistor limits the system voltage including the I/O pads to a typical value of 1.2V.



Irradiation: Samples of the STRV-R1 have been irradiated to at least 500 Mrad of Total Ionizing Dose at a dose rate of 1.75 Mrad/hour. Irradiation has been performed at -10°C and -40°C. A major increase in the leakage current of the SRAM from 60µA to 530µA has been observed at dose of 20Mrad.

No permanent or temporary functional interrupt has been observed in the core or the SRAM cells during the complete irradiation.





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