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STRV –A radiation hard RISC-V microprocessor for high-energy physics application

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Currently microprocessors are precluded from the use in several high-energy physics applications due to the harsh radiation present. The STRV-R1 (SEU-tolerant-RISC-V) RSIC-V microprocessor aims to overcome this limitation and replace the custom digital control logic found in current ASICs. A triple modular redundancy (TMR) based protection scheme is applied to protect the RISC-V microprocessor core and other system components like the SRAM against radiation induced soft errors. The implementation has been done in a 65nm CMOS technology.
The radiation hard architecture of the RISC-V microprocessor is discussed and initial measurements of the first silicon are presented.

Summary (500 words)

The STRV-R1 is a RISC-V microprocessor designed to target the harsh radiation environment present in locations that are close to the beam pipe or the interaction point, such as the ATLAS and CMS detectors installed at the Large Hadron Collider (LHC).
The target is to tolerate a total ionizing dose (TID) of 1 Grad and a high single event effect (SEE) rate due to a particle flux of up to 1.5 GHz/cm2, which current RISC-V implementations do not allow. The use of a microprocessor, as opposed to custom digital logic used in current ASICs, aims to enable faster development cycles through firmware updates rather than extensive redesigns.

The STRV-R1 features a RISC-V core which supports the RV32I ISA variant and has a three stages pipeline. In addition a ISA-extension for accelerated multiplication and division is integrated. The system is intended to run at a base clock frequency of 50 MHz and contains 32 kB of available SRAM for data and instructions. A memory bridge between the core's two buses, the instruction bus and the data bus, and the SRAM allows both buses to access the full SRAM.

The STRV-R1 uses triple modular redundancy (TMR) to mitigate errors caused by SEE. TID effects are targeted through the use of a 65nm fabrication technology in combination with thin gate oxide transistors which achieves an inherently high TID hardness. The fine-grained TMR implemented in STRV-R1 contains a voter after every sequential element. To prevent the accumulation of errors in sequential elements that are not updated every clock cycle, a feedback path is integrated that guarantees that a SEU in a sequential element is corrected within the next clock cycle. The SRAM is protected by triplication of the SRAM blocks which have their output majority voted before the data is transferred to the RISC-V core. Accumulations of SEUs in the SRAM is a major concern since there is no upper time limit between write accesses to a particular row of the memory. To oppose the accumulation of SEUs in the SRAM, the STRV-R1 relies on a self-refresh algorithm that independently from the RISC-V core periodically refreshes the SRAM.

The microprocessor has been implemented in a 65 nm bulk CMOS technology and uses a 1.2V supply voltage level. It is divided into three domains, which allows a finer analysis of the system power consumption. The core domain incorporates the RISC-V core, the debug module, and the memory interfaces. The SRAM domain contains the SRAM cell macros and the scrubbing algorithm. The peripherals domain provides 27 configurable GPIOs, a UART interface and a JTAG-Interface used for programming and debugging of the core. The system also contains counters, which record the number of SEUs detected by the majority voters.

In this talk, the functionality and architecture of the STRV-R1 microprocessor will be presented.The resource penalties of the protection scheme within the RISC-V microprocessor system are discussed, and initial measurements of the first silicon of the radiation tolerant RISC-V microprocessor are presented.

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