Contribution ID: **109** Type: **Poster**

Design and preliminary results of a shunt voltage regulator for a HV-CMOS sensor in a 150 nm process

Tuesday 20 September 2022 16:40 (20 minutes)

The University of Liverpool HV-CMOS R&D group develops depleted monolithic active pixel sensors (DMAPS) for use in high radiation environments. In this contribution, we will present an overview of results from the latest chip, UKRI-MPW0. The contribution will focus primarily on the design of three sub-circuits, a bipolar junction transistor (BJT) based bandgap reference (BGR), a fully CMOS based bandgap reference and a shunt regulator, and their measurement results. The challenges of the analogue design and how they were solved will be discussed.

Summary (500 words)

High-Voltage CMOS (HV-CMOS) sensors are one of the main candidate technologies for future tracking detectors in high luminosity colliders. In spite of their many advantages including material budget, pixel granularity and radiation tolerance, these sensors need further research to boost their performance parameters to meet the challenging requirements of future experiments. UKRI-MPW0 is a proof-of-concept HV-CMOS pixel chip aimed at pushing the performance boundaries of these sensors. This chip implements a novel sensor cross-section optimised for backside biasing to unprecented high voltages to improve radiation tolerance. High breakdown voltages beyond 600 V have been measured before and after irradiation. UKRI-MPW0 contains two active pixel matrices, one with linear transistors and another one with enclosed layout transistors, aimed at testing the novel sensor cross-section. The chip implements, as well, a shunt voltage regulator to generate the various power supply levels locally on-chip to reduce external circuitry and improve the noise performance.

This contribution will focus on the design and performance evaluation of the shunt voltage regulator in UKRI-MPW0. The reference voltage for the regulator is provided by a BJT or a CMOS bandgap reference circuit, both integrated in the chip. The shunt regulator is designed such that an external resistor creates a feedback network allowing the output voltage to be adjusted for different applications. The two bandgap references make use of proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) design components, which cancel each other out and provide an output that is independent of temperature. The BJT bandgap provides a reference voltage of 1.2 V, with a maximum voltage variation of 7 mV across an input range of 1.4 to 1.8V and a maximum voltage variation of 5 mV between -40 ℃ and 120 ℃. The fully CMOS bandgap provides a reference voltage of 350 mV, with a maximum voltage variation of 2 mV across an input range of 0.8 to 1.8V and a maximum voltage variation of 8.4 mV between -40 ℃ and 120 ℃. The combined power consumption of the BGRs is 478.8 µW. The power consumption of the shunt regulator is dependant on the output voltage chosen, and the value chosen for the external shunt resistor. The layout of the circuit, including the bandgaps, is 270 µm x 250 µm. For debugging purposes the voltage regulator can function as a standalone object or to power the active pixel matrices.

The performance evaluation of the voltage regulator and bandgap reference circuits, with respect to variations in input voltage and temperature and in comparison with simulated results, will be presented at the conference. The experimental setup uses a Caribou based DAQ system and a cooling system based on a Peltier and a custom PID temperature-controlled chamber. The bandgaps and shunt regulator have been tested for temperature stability over the range of -25 ºC to +70 ºC, with a maximum voltage variation which agrees

with values expected from simulations. Future measurements are planned after TID irradiation to study the radiation tolerance of the various sub-circuits described.

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Session Classification: Tuesday posters session

Track Classification: ASIC