Future developments of radiation tolerant sensors based on the MALTA architecture

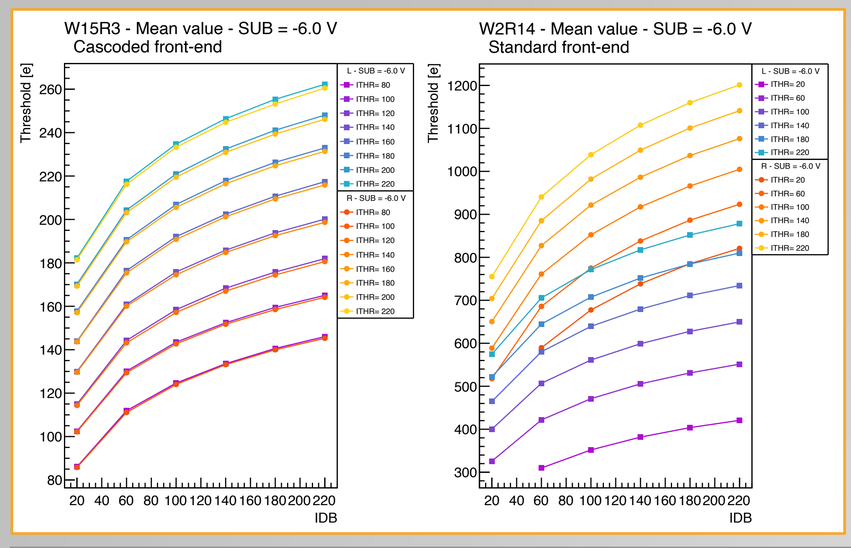
D. Dobrijevic[1,2], T. Suligoj[2] and H.Pernegger[1] on behalf of the MALTA collaboration

1-CERN, Switzerland, 2-University of Zagreb, Croatia

UNIVERSITY OF ZAGREB
Faculty of Electrical Engineering and Computing

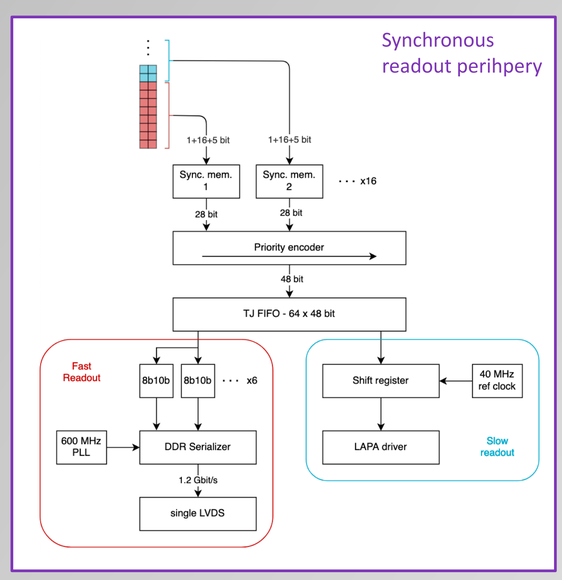
The planned MALTA3 DMAPS designed in the standard TowerJazz 180 nm Imaging process will implement the numerous process modifications, as well as front-end changes in order to boost the charge collection efficiency after the targeted fluence of $1x10^{15}$ MeV N_{eq}/cm^2. The effectiveness of these changes have been demonstrated with recent measurements of the full size MALTA2 chip. With the original MALTA concept being fully asynchronous, a small-scale MiniMALTA demonstrator chip has been developed with the intention of bridging the gap between the asynchronous pixel matrix, and the synchronous DAQ. This readout architecture will serve as a baseline for MALTA3, with focus on improved timing performance. The synchronization memory has been upgraded to allow clock speeds of up to 1.28 GHz, with the goal of achieving a sub-nanosecond on-chip timing resolution. The subsequent digital readout chain has been modified and will be discussed in the context of the overall sensor architecture

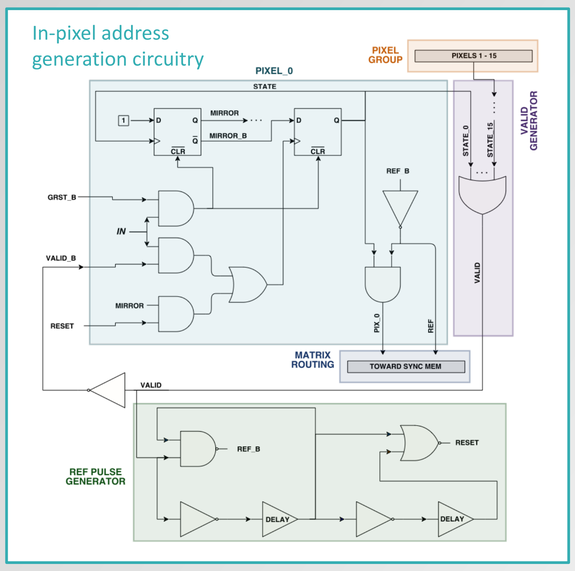
Front-end improvements



- Cascoded front-end exhibits sub 100e⁻ thresholds, with an RMS value of <10e⁻

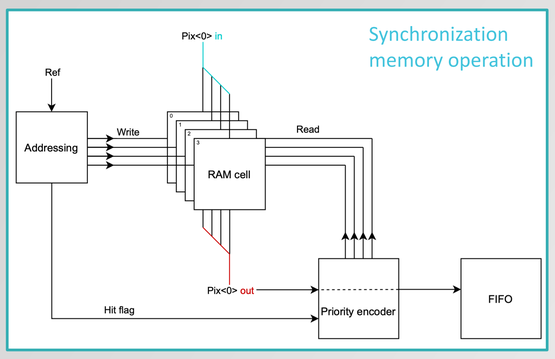
MiniMALTA Architecture

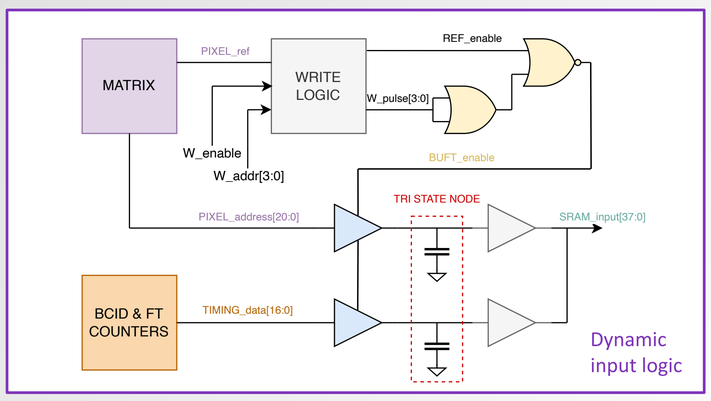




- The **in-pixel address generation circuitry** (shared with all MALTA chips) generates a programmable length pulse immediately after hit detection. Combined with the individual pixel states, an address is generated and sent down a NAND propagation chain.
- The **MiniMALTA synchronous periphery** is focused around the Synchronization memory array – a 640 MHz clocked block which latches incoming asynchronous hits from the matrix, while appending the BCID and fine time of the given event.
- These hits are passed to the priority encoder and stored in a standard FIFO. They are subsequently read out using either the default readout circuitry and a 1.28 Gbps serial link, or an auxiliary 160 Mbps module

MALTA3 Synchronization memory

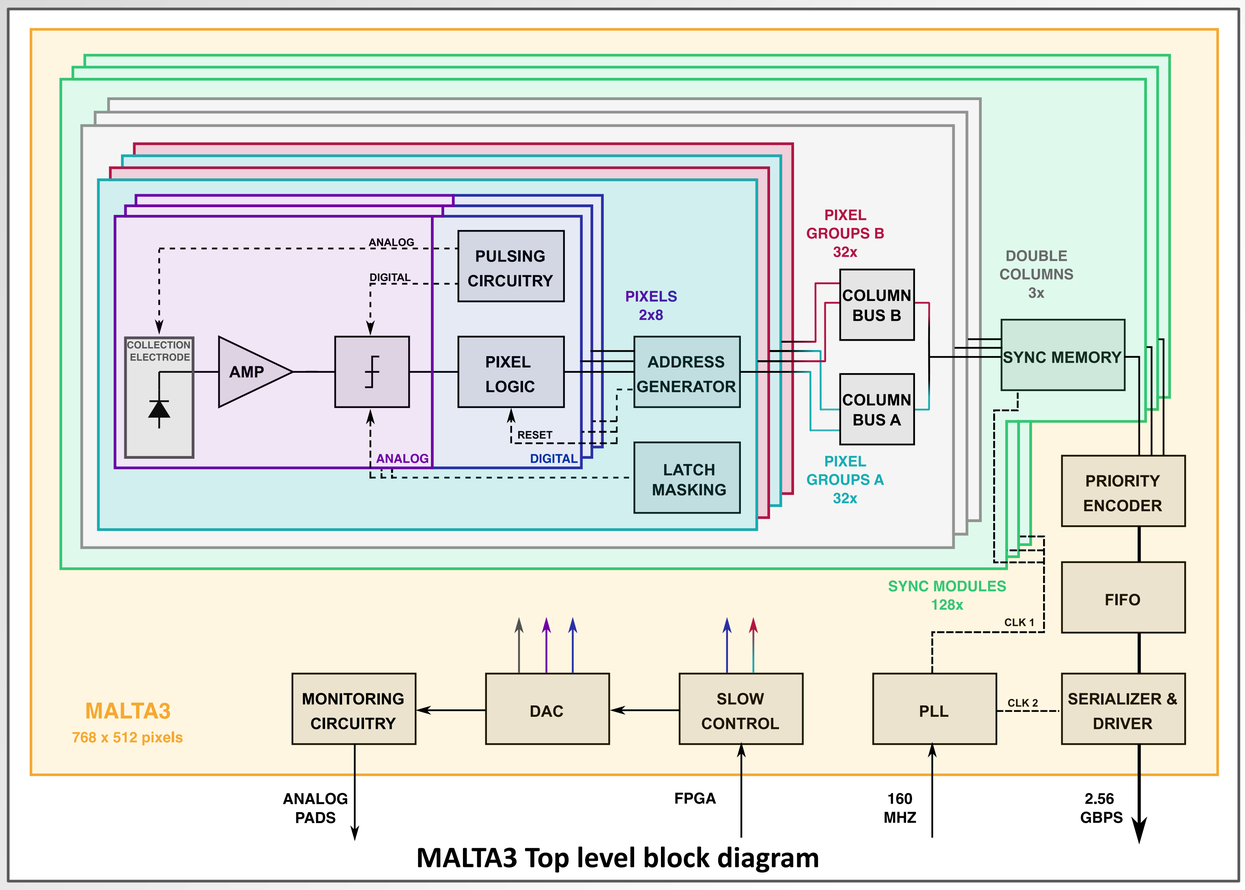




- The encoded twisted ring counter serves as the foundation of the new synchronization memory. In order to ensure proper operation at 1.28 GHz, custom logic was devised for the Gray encoder and the ring itself.
- Previous MiniMALTA iterations used duplicated write generation logic instead of input buffers so timing of both the input address and the write signal can be equalized. It was replaced by tri-state dynamic input logic, reducing the time window in which the incoming information can change, and increasing precision.
- Due to usage of a custom dual port SRAM array, write and read actions can occur at the same time in the synchronization memory, as long as the same cell is not accessed for both operations at once

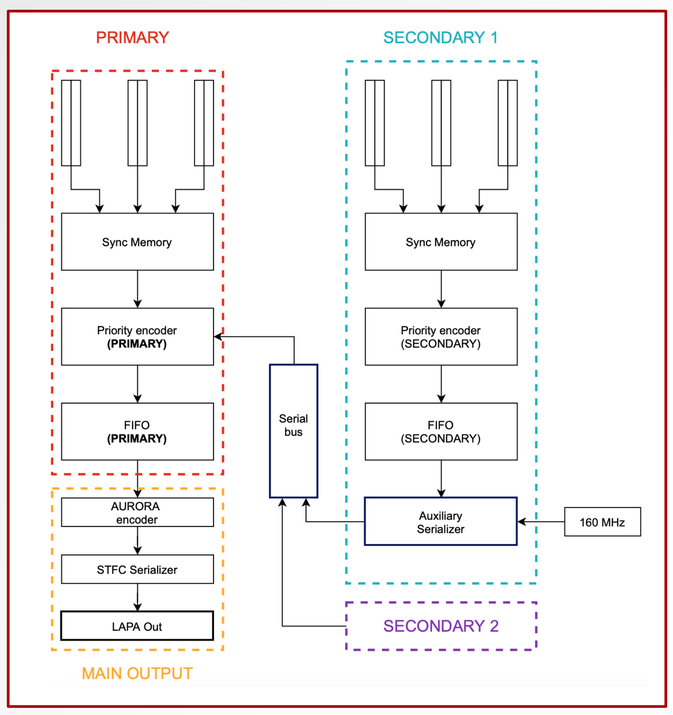
MALTA3

- The new design will use a conceptually identical matrix, in a slightly different format (768x512 pixels)
- An on-chip PLL is used to generate the 1.28 GHz clock, used both for the Synchronization memory and the main output serializer. Aurora encoding will be the last stage before the serializer.
- The slow control will use a standard I2C protocol, instead of the previous shift register based design



MALTA3 Top level block diagram

Future outlook



- The asynchronous merging concept used in previous MALTA chips is not compatible with the new synchronous digital periphery
- Current parallel CMOS drivers used for chip-to-chip data transfer could be reutilized as multiple independent serial links
- The priority encoder would need to have a configurable serial receiver – **internally treated as an additional column**
- An Auxiliary serializer is to be inserted after the last FIFO stage - if configured, all data would be steered through this channel
- The main chip would be configured to take in additional data through the modified priority encoder – **the rest of the chain would remain the same**

Conclusion

- Previous MALTA iterations focused on increasing the charge collection efficiency and radiation hardness through front-end and process modifications
- Recent MALTA2 measurements demonstrated a 97.5% charge collection efficiency after $2x10^{15}$ MeV N_{eq}/cm^2, prompting further development focus more on timing performance
- A small scale demonstrator, the MiniMALTA3, is in the final stages of design. The goal is to verify the upgraded synchronization memory before it could be integrated on a full scale chip
- This design is intended to be modular, so a full-chip expansion of this architecture can be more straightforward

References

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