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Maintaining data integrity in a cryogenic SoC ASIC driving 25 m cable at 160K and 87K with gigabit data rates

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The ASICs for charge readout of the DUNE and nEXO experiments will operate under noble liquid environments and will transmit data over long cables (up to 25 m). We have designed a custom LVDS transmitter to cope with the cable insertion loss and maintain data integrity. The transmitter features a tunable pre-emphasis circuit and bias current, which allows us to drive different cable lengths at cryogenic temperatures. We will present the characterization and modeling of the cable insertion loss, the design of the custom LVDS driver, and the comparison of eye diagrams at various frequencies and temperatures.

Summary (500 words)

An essential component for neutrino experiments such as Deep Underground Neutrino Experiment (DUNE) and next Enriched Xenon Observatory (nEXO) is the Time Projection Chamber (TPC). These large detectors operate at cryogenic temperatures (i.e., LAr at 87K and LXe at 160K) and deposit a charge signal in the detector wires when neutrinos interact with noble liquids. A cryogenic system-on-chip (SoC) ASIC has been designed to collect this charge, digitize and processed using a reliable data acquisition system.

Read-out of the cryogenic ASIC becomes unique as the electronics are directly submerged in noble liquids in a TPC located deep underground. However, the data acquisition on the warm side of the experiment is above ground and therefore, long cables are required for the read-out. For DUNE and nEXO experiments, these cable lengths range up to 25 m while transmitting data at approximately 1 Gbps. For the DUNE experiment at 87K, SAMTEC Twinax cable (see Fig. 1.a) is used for data transmission. To calculate the dB loss introduced by cable, mixed-mode S-parameters were measured with a 4-port vector network analyzer (VNA). Four-port network analyzer evaluates the value of the S-parameter at all 4 nodes. They are named S11, S12, S21, and S22, respectively. Furthermore, these parameters vary with frequency. At 1 GHz, 20 dB insertion loss could amount to roughly 10 times in amplitude reduction (i.e., 20 dB = 20*log10(Vout/Vin)). The final paper would describe the methods and formulae to calculate the actual values of the insertion loss by Twinax cable at a target frequency.
For the loss of data integrity due to cables, an on-chip pre-emphasis circuit is designed along with the increased bias current in the main LVDS transmitter (see Fig. 1.b). This circuit provides an additional output current during fast transition times of the signal. This tends to speed up the edge rate and provides a bit of overshoot to the signal at the driver output. The injection of current of the pre-emphasis is controlled by a delay circuit that can be programmed through a dedicated control-unit interface. The delay ranges from 1 ns to 3 ns with steps of 500 ps. The pre-emphasis circuit can be also enabled or disabled through a bit control using the control-unit interface. The main LVDS driver, on the other hand, provides currents up to 15 mA. The LVDS is fully programmable and has been optimized to operate in cryogenic environments using custom models, which allows driving different cable lengths (up to 25 m) across temperatures. This combined signal conditioning method helps to restore the total output voltage swing for proper synchronization of the data for read-out. The final paper plots the eye diagram and does a comparative analysis of the output voltage swing for the data at various frequencies at room and cryogenic temperatures.

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