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A Low-Power 1 Gb/s Line Driver with Configurable Pre-Emphasis for Lossy Transmission Lines

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A line driver with configurable pre-emphasis is implemented in a 65nm CMOS process. The driver utilizes a three-tap Feed-Forward Equalization (FFE) architecture. The relative delays between the taps are selectable in increments of 1/16th of the Unit Interval (UI) via an 8-stage Delay-Locked Loop (DLL) and digital interpolator (DI). One can also control the output amplitude and source impedance during each UI via a programmable array of eight Source-Series Terminated (SST) drivers. The entire design, consisting of the DLL, two DIs, and three SST driver arrays, consumes 7.2mW from a 1.2V supply (67% from the SST drivers) at 1Gb/s.

Summary (500 words)

Modern front-end ASICs require line drivers to send the digitized measurement data off-chip. Such line drivers must be optimized for the specific transmission line (i.e., cable) used by the system to ensure a low Bit Error Rate (BER) while also minimizing power consumption. However, conventional driver architectures based on Current-Mode Logic (CML) consume significant amounts of power (typically, more than 20mW) to obtain adequate signal swings. In addition, they do not allow the output waveform to be optimized for a given cable, i.e., their pre-emphasis parameters are not configurable. Pre-emphasis or Feed-Forward Equalization (FFE) is a technique in which the BER is minimized by filtering the transmitted waveform with the inverse of the cable Transfer Function (TF). Since the latter is usually low-pass, the pre-emphasis function is usually high-pass. It is generally implemented using a Finite Impulse Response (FIR) filter in which the taps have fixed relative time delays of 1 Unit Interval (UI) and adjustable weights. However, approximating the desired TF using such fixed tap delays is challenging, thus preventing the BER from being minimized for a given cable. To address this issue, we develop a line driver that enables fully configurable pre-emphasis functions via an eight-tap Delay-Locked Loop (DLL) and Digital Interpolator (DI) and is capable of operating at any temperature between LN2 (77K) and room temperature. A top-level block diagram of the design is shown in Figure 1. The pre-emphasis is implemented using three taps (denoted by pre-tap, main-tap, and post-tap) with user-programmable time delays. The DLL uses a Phase Detector (PD), Charge Pump (CP) and Voltage-Controlled Delay Line (VCDL) to create a negative feedback loop for accurately setting these delays in the presence of Process-Voltage-Temperature (PVT) variations. A false lock detector monitors the VCDL output taps to ensure that the DLL locks to the correct operating point (Vc). A replica VCDL reuses the Vc voltage to create eight copies of the input data with relative delay of UI/8. These outputs are further processed by a tap selector circuit that allows the user to either select one output or digitally interpolate between two adjacent outputs. Hence, the relative time delays between the pre-emphasis taps can be programmed to one of sixteen values (in steps of UI/16). Each tap is fed into a parallel array of eight Source-Series Terminated (SST) drivers with configurable unit currents, such that the relative weights of the taps can be programmed via the number of drivers that are enabled. The weighted driver outputs are then summed to generate the final output waveform (see Figure 2a). The SST drivers have 2 to 4 times lower power consumption than conventional CML drivers, but also have weight-dependent output impedance (thus introducing inter-tap loading effects that can be compensated by adjusting the tap weights). Running at 1 Gb/s over a high-loss cable of 3m length (attenuation of -19dB at 1GHz, see Figure 2b) at room temperature, the driver provides an adequate eye opening (0.72UI and 202.6mV, see Figure 2c) without error correction while consuming only 7.2mW.

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