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The monolithic ASIC of the high-resolution pre-shower of the FASER experiment

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A high resolution W-Si preshower detector is proposed for the FASER experiment at CERN to enable the measurement of new physics signals related to Long Lived Particles. For this purpose, a 1.5x2.2 cm2 monolithic silicon active-pixel detector is being developed. The detector will integrate ultra-fast, low-noise front-end electronics in 65 μm side hexagonal pixels. The system is designed to read out thousands of pixels per event. Three pre-production ASICs in 130 nm SiGe BiCMOS technology were submitted for fabrication to test the best design solution for the final chip.

Summary (500 words)

The main goal of the FASER experiment at CERN is the search for dark matter through the detection of low-mass Long-Lived Particles (LLP), extending the physics program of the other experiments at the LHC. While the current FASER detector can measure with high precision electron-positron pairs produced by the decay of dark photons, it has not the granularity to measure e.g. two-photon final states. For this reason CERN has recently approved the construction of a W-Si pre-shower that will make the experiment able to discriminate the signal from two photons separated by 200 μm with energies ranging from 100 GeV to few TeV, thus extending the discovery potential of FASER to neutral final states.

A monolithic silicon active-pixel sensor is being developed for the new pre-shower. The ASIC, a 1.5x2.2 cm2 full reticle chip with 65 μm side hexagonal pixels, will be produced in 130 nm SiGe BiCMOS technology. The hexagonal shape was chosen to reduce the peak electric field at the edges of the active area of the pixels. The specification of the project requires the possibility of measuring the charge of each individual pixel to reconstruct the profile of the ultra-collimated electromagnetic showers. Because of the high pixel density and the efficiency specification, the integration in pixel of ultra-fast, low-noise and low-power front-end electronics is required. A first prototype ASIC demonstrated the possibility of integrating the front-end inside the pixel while preserving stability and meeting the target performance of <200 electrons Equivalent Noise Charge at a power density of <150 mW/cm2.

A pre-production ASIC which integrates the main characteristics of the final chip has been designed. The ASIC is divided in super-columns made of 8 blocks of 16x16 pixels, indicated as super-pixel. The pre-production chip has been designed in three versions, featuring different front-end and readout configurations. The charge collected by each pixel during an event is measured by charging a large capacitor in pixel with a constant current during the signal time-over-threshold. Each super-pixel will use a 256-to-1 analog multiplexer and a 4-bit flash ADC to convert the charges in a frame-based readout operating at 200 MHz.

The super-columns are split in half by the super-column logic, a digital system including a logic to mask the pixels, to generate the test-pulses and handle the polling process for the conversion of the charges during the readout. The super-column logic spans almost the entire chip with a length of approximately 1.4 cm, but it is only 37.7 μm wide to reduce the dead area. Dedicated design techniques were developed to achieve the physical implementation of the readout logic with this challenging aspect ratio.

An additional digital logic integrated in the periphery of the ASIC handles the programming phase and the readout. The latter is characterized by a super-column-level frame-based design that was chosen to minimize the readout time.

The results of the tests performed on the pre-production prototypes will determine the optimal front-end configuration and the design for the 13 super-column final chip of the experiment.

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