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The irradiation test and upgrade of the Gigabit Transceiver For The ATLAS Inner Tracker Pixel Detector Readout Upgrade

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This paper presents the irradiation test results and a revised design of a gigabit transceiver, GBCR, for the ATLAS Inner Tracker (ITk) Pixel detector readout upgrade. The GBCR includes 7 receiver channels operating at 1.28 Gbps and two 160 Mbps transmitter channels. The transmitter and receiver channels connect to the front-end readout chip via 34-American Wire Gauge (AWG) twin-axial cables up to 5 meters and a 1-meter flex cable. After we found the chip was SEE sensitive in an irradiation test, we submitted a revised design in February and expected to get the test results this summer.

Summary (500 words)

In the ATLAS inner tracker (ITk) Pixel Detector Phase-II upgrade, low-mass cables between the detector and the Optical Box induce significant Inter-Symbol Interference (ISI) due to the high-frequency signal loss over the cables. The upstream data rate is 1.28 Gbps and the signal loss at its Nyquist frequency is about 10 dB. The signal does not meet the lpGBT receiver specification. To overcome the problem, the GBCR is designed for receiving data from the frontend readout ASIC, RD53 and regenerating the data for optical link transmission. Meanwhile, the GBCR also provides transmitter channels to reduce the ISI jitter on 160 Mbps command signals, from which RD53 recovers the clock.

GBCR has 7 upstream receiver channels and two downstream transmitter channels. Each upstream channel receives 1.28 Gbps data through 34-AWG twin-axial cables up to 5 meters and deliveries the recovered data to the lpGBT on an optical board. Each receiver channel consists of an equalizer, retiming logic, a limiting amplifier, and an output driver. The retiming clock is from an on-chip phase shifter shared by all channels. In the equalizer mode, the phase shifter and retiming logic are off and the equalized signal is sent to a differential output driver. In the retiming mode, the recovered signal is re-sampled by a phase programmable clock signal. In this case, the output signal jitter is determined by the sampling clock jitter. The transmitter channels provide a pre-emphasis function with two CTLE stages.

In the lab test, the receiver channels work as we expected in both the equalizer and retiming modes. The recovered signal jitter meets the lpGBT requirements, less than 200 ps. The transmitter channel improves the input signal jitter but it is below expectations. In a preliminary radiation test, we observed various SEE errors. To confirm further the results, we booked a beam test for a second radiation test in May this year. We simulated the design with charge injection and found that the equalizer and the passive attenuator are sensitive to potential SEE events. The critical charge in the equalizer is 2 fC only. We removed the attenuator and triplicated the equalizer in receiver channels. We have a multiplexer to select the output signal from triplicating signals, voted signals, or retimed signals, corresponding to 3 working modes: test, equalizer, and retiming modes. We also improved the transmitter channel design by fine-tuning the CTLE RC network. Although we remove one receiver channel because the triplication of equalizers takes more area than the previous design, we keep the remained channels with the same pins as the previous design so that we can reuse the test board and current optical board.

The revised GBCR design was submitted in February, and we expect to test the chips before the TWEPP meeting in September.

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