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# Second generation Monitoring of Pixel System (MOPS) chip for the Detector Control System (DCS) of the ATLAS ITk Pixel Detector

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The Monitoring of Pixel System (MOPSv2) chip is an Application Specific Integrated Circuit (ASIC) foreseen to provide the temperature and the voltage monitoring data of individual front-end detector modules to the Detector Control System (DCS) of the ATLAS ITk Detector.The chip is required to be radiation hard up to an ionizing dose of 500 Mrad, immune to Single Event Upsets (SEUs) and work reliably at high operating temperatures of up to 40 degrees. In this talk, the functionality / performance of the second version of the chip will be discussed, and also results
from the irradiation campaigns will be presented.

## Summary (500 words)

The High Luminosity (HL) upgrade for the Large Hadron Collider (LHC) at CERN will provide a 10x increase in the integrated luminosity. The ATLAS experiment will get a completely new all-silicon Inner Tracking Detector (ITk) during the phase-II upgrade to work with the new HL-LHC. The innermost part of the ITk is the Pixel detector consisting of 5 layers and more than 10k detector modules. The new Pixel Detector will use serial power chains with a maximum of 16 readout modules in a single chain to reduce services inside the detector.
The Monitoring of Pixel System (MOPSv2) chip is an Application Specific Integrated Circuit (ASIC) and an improved version of the MOPSv1 foreseen to provide the temperature and the voltage monitoring data of the individual front-end detector modules, which are operated in a serial powering chain, to the Detector Control System (DCS) of the ATLAS ITk Pixel Detector. The chip is built using a 65nm CMOS process and dimensions of 2x2 mm2. The Total Ionizing Dose (TID) requirement for the chip is 500 Mrad. Due to the high radiation environment, the chip is required to be immune to the Single Event Effects (SEEs), particularly Single Event Upsets (SEUs) where a stored bit can flip due to charge accumulation. The on-chip 32-channel 12-bit ADC provides the possibility to measure module supply voltage using a simple voltage divider network and the temperature by an NTC sitting on the readout modules in the serial power chain. The reference voltage for the NTCs is also provided by the MOPS chip. The chip communicates using the standard Controller Area Network (CAN) digital protocol and a custom low voltage physical layer of 1.2 Volts. On the application layer, the chip implements a limited application-specific part of the CANopen standard which also requires an Object Dictionary (OD) defined in the hardware. Another important feature of the MOPSv2 is that it provides the functionality of automated oscillator trimming to compensate for chip variations which can cause frequency mismatch on the communication bus. The automated trimming is not a part of the standard CAN / CANopen standards.
To make the chip immune to SEUs, Triple Modular Redundancy (TMR) has been used in conjunction with some other techniques to mitigate different scenarios which can make a power cycle inevitable. SEU immunity is important to preserve data integrity and to assure reliable operation of the chip by avoiding frequent power cycling.
The chip has been irradiated with critical low dose rates of 40 Krad / hour to accumulate the TID of 33

Mrad. High operating temperatures of up to 20 and 40 degrees Celsius have been used during the X-ray irradiation campaigns. The chip has proven to work reliably during irradiation and at 60 degrees Celsius after the TID of 500 Mrad. To test SEU immunity, the chip has been irradiated at a heavy-ion facility in CRC UCLouvain.

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