Design and readout architecture of a monolithic binary active pixel sensor in TPSCo 65nm CMOS imaging technology

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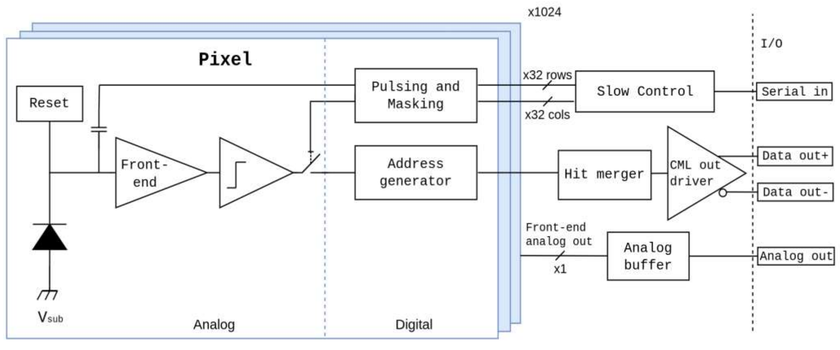
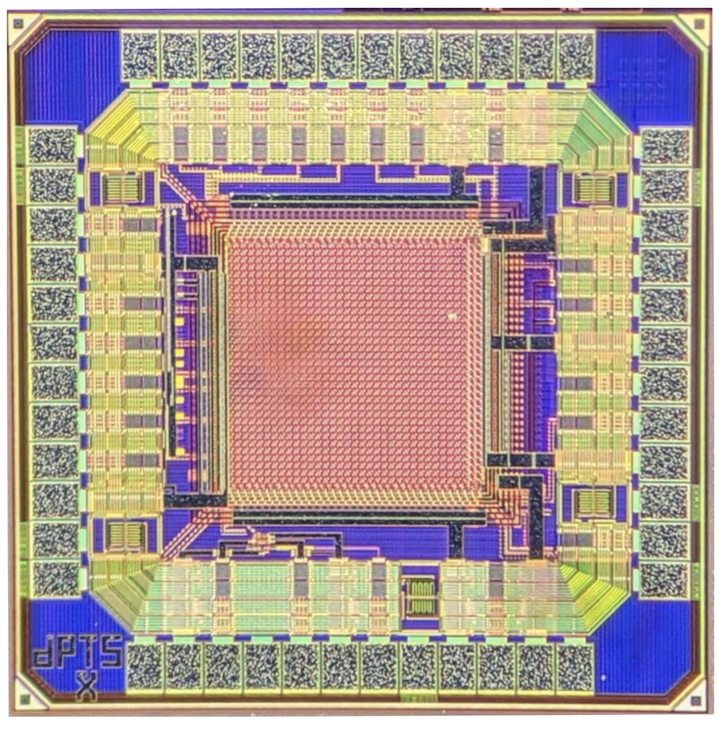
The Digital Pixel Test Structure (DPTS) is a monolithic active pixel sensor prototype chip designed to explore the TPSCo 65nm ISC process in the framework of the CERN-EP R&D on monolithic sensors and the ALICE ITS3 upgrade. It features a 32x32 binary pixel matrix at 15 µm pitch with event-driven readout, based on GHz range time-encoded digital signals including Time-Over-Threshold. The chip proved fully functional and efficient in testbeam allowing early verification of the complete sensor to readout chain. The focus is on the design and in particular the digital readout and its perspectives with some supporting results

Chip functional diagram

The DPTS features masking and digital capacitive pulsing for each pixel, together with a single CML output for time-encoded hit data and a single analog monitor output interfaced with the front-end circuitry

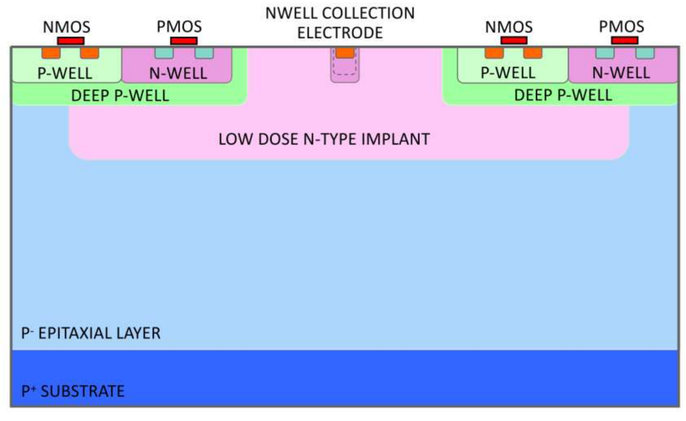




1.5 mm

Pixel Sensor

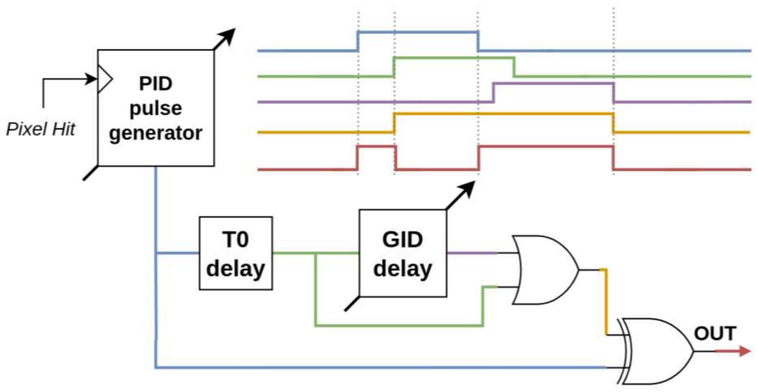
Sensor designed for charge collection optimization. A gap is inserted between the pixels electrode to increase lateral field. The depletion is achieved by reverse bias of the substrate



sensor structure similar to 180nm TowerJazz in [3,4]

Asynchronous Event-Driven Readout Circuit

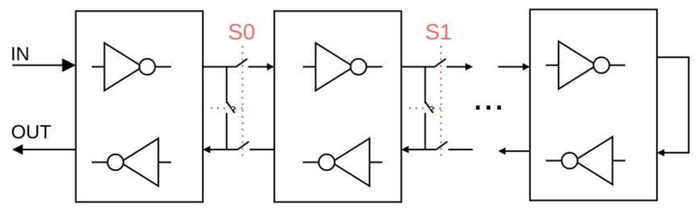
Hit position is encoded in a train of 2 pulses, sent twice at ToT interval. The digital readout organized by independent groups (columns) of 32 pixels each. Each group features a fixed GID delay to encode its position, while the position of the pixel in the group is given by a Pixel ID pulse generator that also initiates the hit-driven transmission. The nominal time encoding resolution for PID and GID is 150ps.



Readout diagram for a group (column) of 32 pixels

Group ID delay

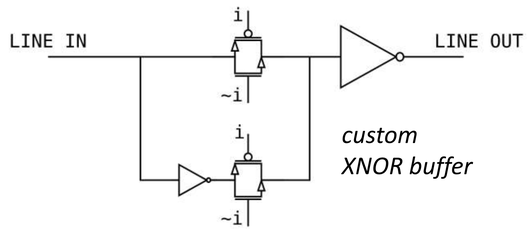
The group ID (GID) delay is set for each group of pixels by hardwiring a one-hot encoded configuration of the S0..S31 switches of a programmable delay ladder structure based on CMOS inverters

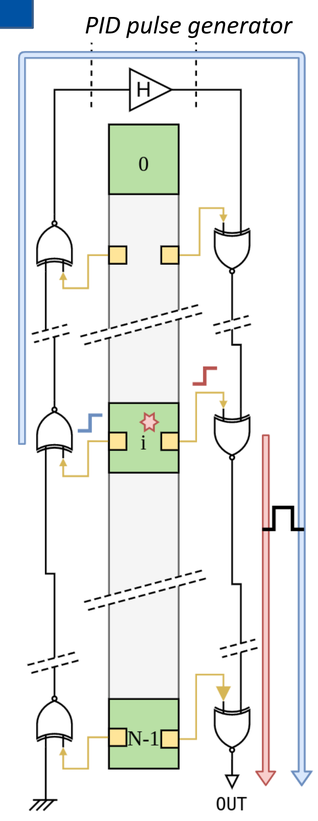


Group ID programmable delay chain

Pixel ID pulse

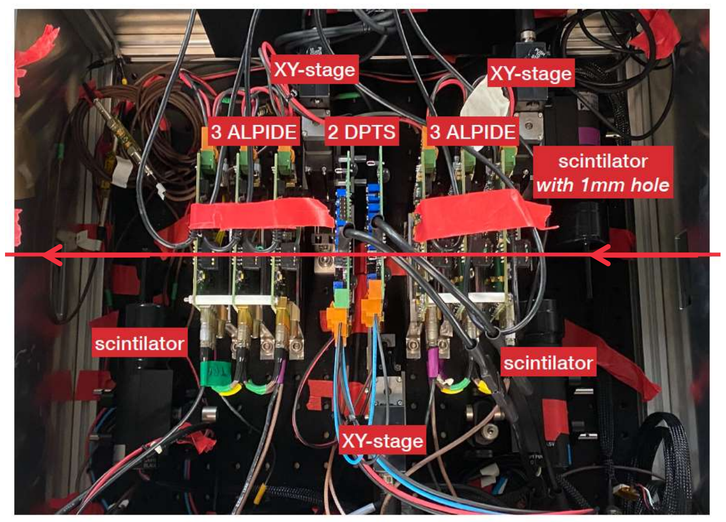
An original monostable circuit, distributed over a group of pixels (based on full custom XNOR gates) is capable of generating pulses with a duration dependent on the pixel position in the group (PID).
The pulse is formed injecting simultaneously two transitions in specular positions over a folded XNOR delay line.

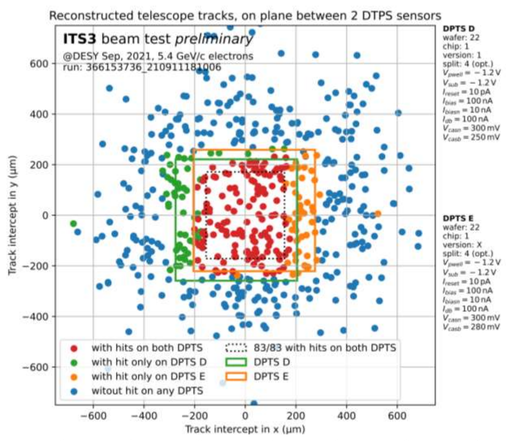




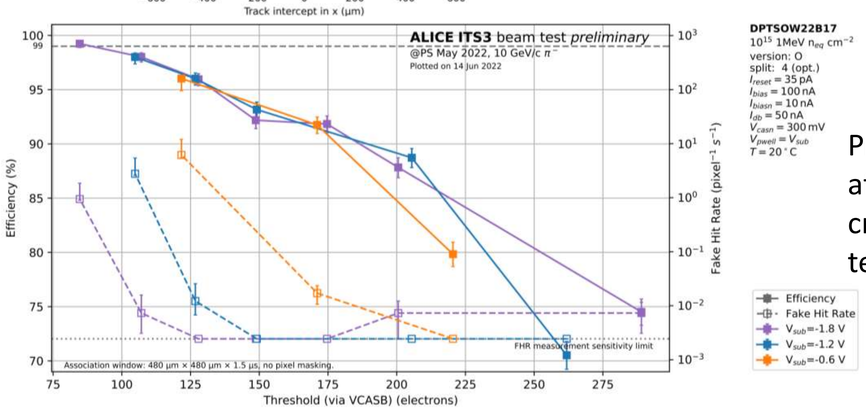
Tests and Results

Beam testsing of two DPTS chips with a scintillator to veto tracks far from area of interest



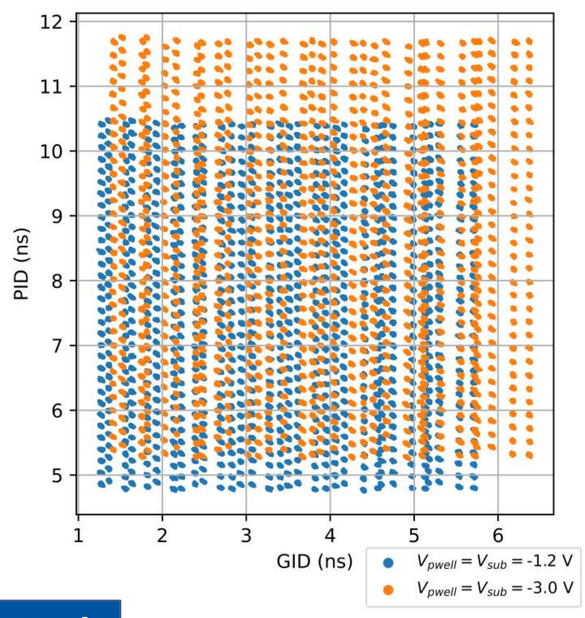


Early results with few hundered tracks showed: Detection Efficiency of 100% $^{+0\%}_{-1\%}$ [95% conf. CP]



Proved fully efficient after 10^{15} MeV n_{eq} cm^{-2} at room temperature !

Distinguishible clusters from repeated pulsing of single pixels: decoding is possible although depending on chip supply, temperature and substrate bias



References

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[2] M. Mager. Ep detector seminar CERN. 2022.
[3] W. Snoeys et al., NIM A 871 (2017) 90
[4] M. Munker et al., 2019 JINST 14 C05013

Future Work

Work is in progress to improve robustness for larger scale sensors. Detailed studies on mismatch, power supply, noise, architectures and tolerance to manufacturing defects are ongoing.