First Measurement Results for the front-end circuits of the Ultra-fast High Pitch digitizer System on a Chip (HPSoC) ASIC

The 4-channel High-Pitch-digitizer-System-on-a-Chip ASIC (HPSoC) (Fig. 1) has been manufactured in 65 nm CMOS by TMSC. It consists of a Trans-Impedance Amplifier (TIA) with an optional voltage gain stage (VGS) of gain 3.3 as analog frontend followed by a waveform digitization system. It has been optimized for thin 20 to 50 um thick AC-LGAD. Their critical signal characteristics are shown in Table 1, indicating the boosted pulse height and very short rise times. Their readout is sparse (500 um pitch, 200 um pads with), leading to the design goals of Table 2.

A photograph of the manufactured ASIC is shown in Fig 1.b. The ASIC was attached to a PCB and the output pulses read out via high-speed probes into a fast oscilloscope. The evaluation of the TIA was done first with calibration pulses. Fig. 2 compares the output shape of the simulated calibration pulse with the measured shape.

The calibration curve between output Pmax and the input voltage (Fig. 3) shows a linear response of the TIA both with and without VGS, with the VGS supplying a gain of 3.3 without appreciable increased noise.

The response of the TIA to β-particles was measured with the ASIC (without VGS) wire-bonded to a 60 um thick 3x3 FBK AC-LGAD array (500 um pitch, 200x200 um^2 metal pads, capacitance ~ 120 fF) as shown in Fig. 4 . Fig. 5.a shows a typical pulse shape indicating excellent rise time Trise and low noise N from the baseline RMS. The rise time shown in Fig. 5.b has a mean of 677 ps.

Data was taken at settings of the oscilloscope range (10 mV/cm) with a bandwidth of 500 MHz and noise contribution of 1.0 mV (to be subtracted in quadrature from the measured value). Fig. 6 shows the jitter vs pulse maximum Pmax.

To compare the jitter with the goals in Table 2, the fitted values of Fig. 6 were divided by 60/50 to account for the longer rise time of the 60 um sensor, and divided by 3.3 for the case that the 2nd gain stage VGS is implemented. In Fig. 7 the combined correction factor of 0.25 has been applied demonstrating jitter down to 10 ps.

Table 1 MIP Signal Characteristics

LGAD Characteristics	50 um	20 um
Rise Time (10-90%) [ps]	455	182
Input Charge (G = 20) [fC]	11	4.6
I_{MPV} Input Current [uA]	15	15

Table 2 ASIC Design Goals

ASIC Parameter	50 um Sensor	20 um Sensor	Comment
Rise time (10 – 90%) [ps]	455	182	Rise time (electronics) = Rise time (sensor signal)
Jitter [ps]	10	5	< 30 % of the predicted "Landau" Noise
S/N	> 50	> 40	S/N = Rise Time / Jitter
Voltage signal [mV]	70	70	$V_{MPV}=R_{FB}*I_{MPV,}$ [R_{FB} = 5 kΩ]
Noise RMS [mV]	1.4	1.8	N = S/(S/N)
Internal Sensor Gain	> 20	> 20	

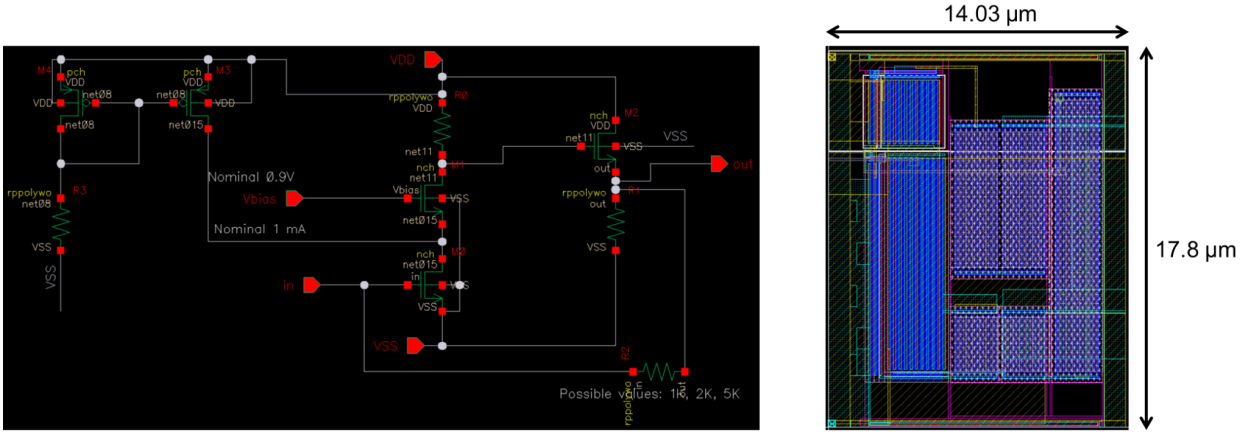

Fig. 1.a Schematic (left) and layout (right) of the TIA

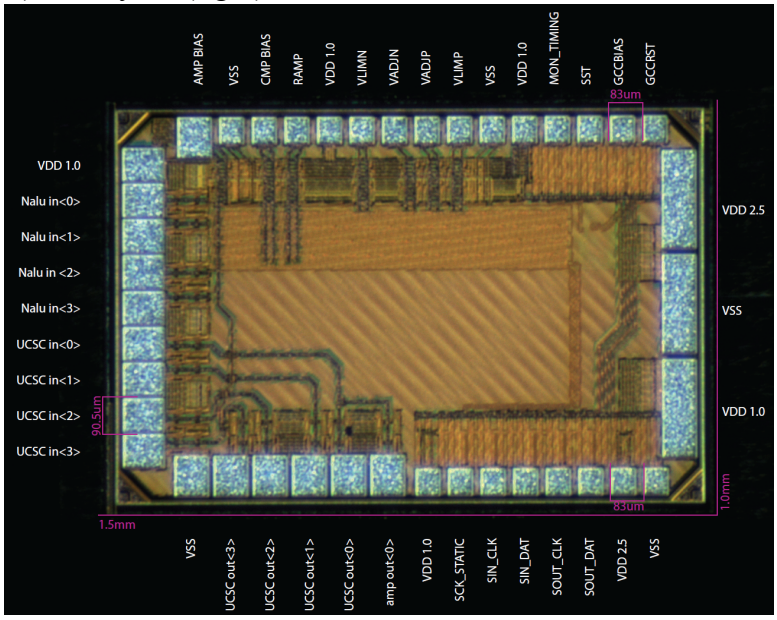

Fig. 1.b Micrograph of fabricated HPSoC prototype chip with labeled pads - the chip is 1.5mmx1.0mm - note the larger pads for the input and test output of the transimpedance amplifiers on the left hand and the power supply rails on the right hand.

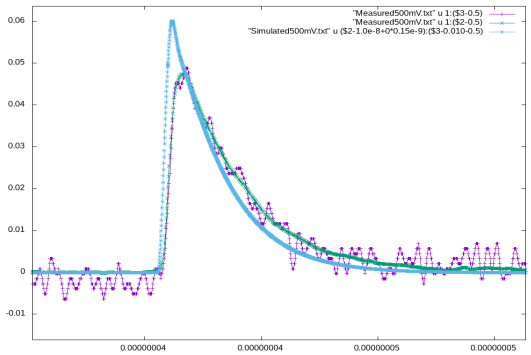

Fig. 2 Output of TIA - measured versus simulated response to calibration pulse

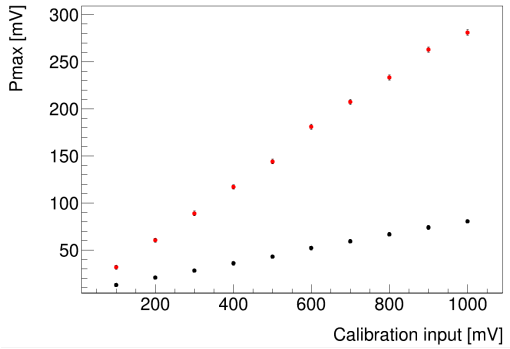

Fig.3 TIA gain measurement: Response without VGS (black), and with VGS (red)

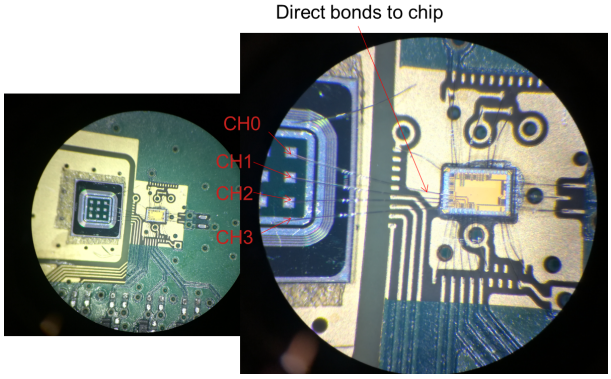

Fig. 4 Test board with AC-LGAD sensor wire-bonded to HPSoC prototype ASIC

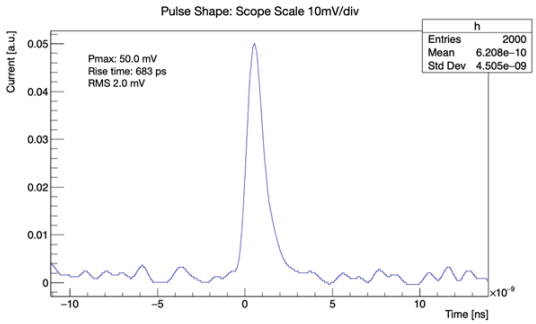

Fig 5.a Typical output pulse from a beta-particle

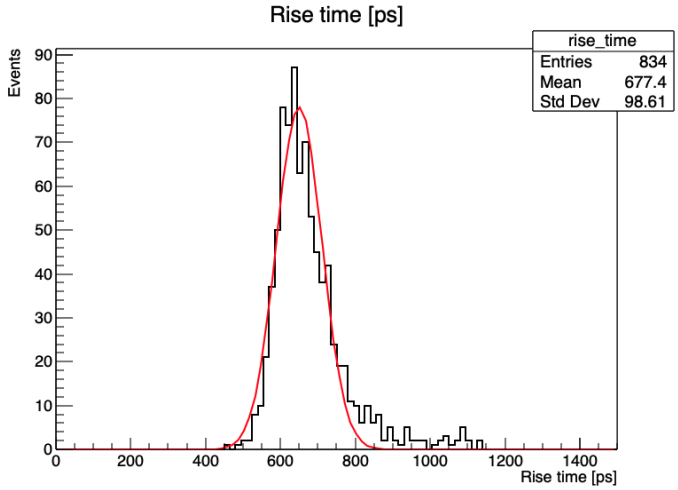

Fig 5.b Rise time with a mean of 677 ps

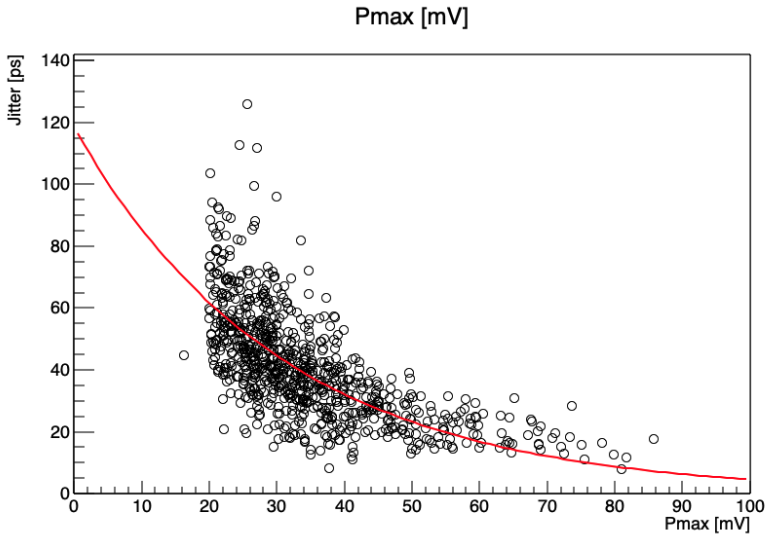

Fig 6. Jitter vs. Pmax after oscilloscope noise corrections

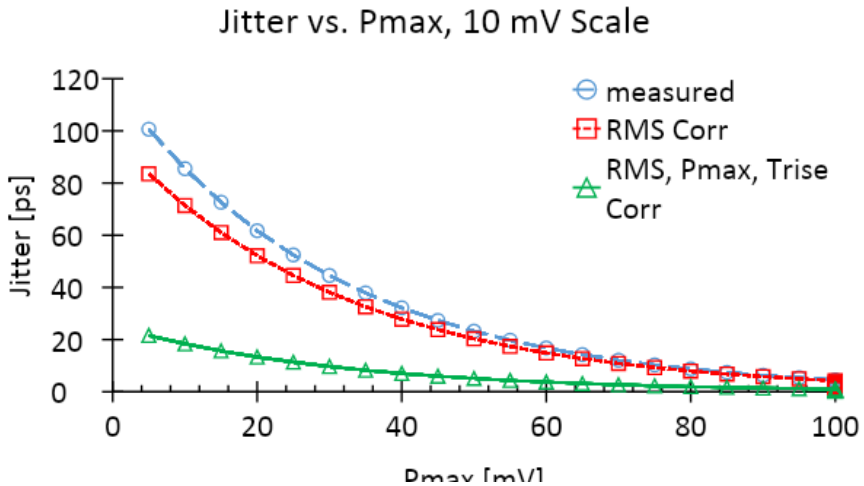

Fig 7. Jitter vs Pmax including corrections for scope noise, sensor thickness and internal amplifier VGS