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First Measurement Results for the front-end circuits of the Ultra-fast High Pitch digitizer System on a Chip (HPSoC) ASIC

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We present the first results from the HPSoC ASIC designed for readout of Ultra-fast Silicon Detectors. The 4-channel ASIC manufactured in 65 nm CMOS by has been optimized for 50 um thick AC-LGAD. The evaluation of the analog front end with β-particles impinging on 3x3 AC-LGAD arrays (500 um pitch, 200x200 um2 metal) confirms a 564 ps output rise time, and a projected jitter value on the order of 10 ps.
We will report on additional tests when using the 2nd stage VGS, a 20 um thick AC-LGAD, the power consumption, and the digital switched-capacitor back-end.

Summary (500 words)

The 4-channel High-Pitch-digitizer-System-on-a-Chip ASIC (HPSoC) (Fig. 1) has been manufactured in 65 nm CMOS by TMSC. It consists of a Trans-Impedance Amplifier (TIA) with an optional voltage gain stage (VGS) of gain 3.3 as analog frontend followed by a waveform digitization system. It has been optimized for thin 20 to 50 um thick AC-LGAD. Their critical signal characteristics are shown in Table 1, indicating the boosted pulse height and very short rise times. Their readout is sparse (500 um pitch, 200 um pads with), leading to the design goals of Table 2.

A photograph of the manufactured ASIC is shown in Fig 1.b. The ASIC was attached to a PCB and the output pulses read out via high-speed probes into a fast oscilloscope. The evaluation of the TIA was done first with calibration pulses. Fig. 2 compares the output shape of the simulated calibration pulse with the measured shape.
The calibration curve between output Pmax and the input voltage (Fig. 3) shows a linear response of the TIA both with and without VGS, with the VGS supplying a gain of 3.3 without appreciable increased noise.
The response of the TIA to β-particles was measured with the ASIC (without VGS) wire-bonded to a 60 um thick 3x3 FBK AC-LGAD array (500 um pitch, 200x200 um2 metal pads, capacitance ˜ 120 fF) as shown in Fig. 4 . Fig. 5.a shows a typical pulse shape indicating excellent rise time Trise and low noise N from the baseline RMS. The rise time shown in Fig. 5.b has a mean of 677 ps.
Data was taken at settings of the oscilloscope range (10 mV/cm) with a bandwidth of 500 MHz and noise contribution of 1.0 mV (to be subtracted in quadrature from the measured value). Fig. 6 shows the jitter vs pulse maximum Pmax.
To compare the jitter with the goals in Table 2, the fitted values of Fig. 6 were divided by 60/50 to account for the longer rise time of the 60 um sensor, and divided by 3.3 for the case that the 2nd gain stage VGS is implemented. In Fig. 7 the combined correction factor of 0.25 has been applied demonstrating jitter down to 10 ps.

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