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BigRock, a Fast Timing Front End for Future Pixels in a 28 nm CMOS Process

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A high-speed, low-power analog front end (AFE) utilizing a current-mode signal path has been designed for 4D tracking applications where precision time resolution of order 50 ps is a requirement. The preamplifier concept is based on a prior art current-feedback CMOS topology [1]. The power consumption of the AFE is 6 uA at 0.9 V process voltage. An on-chip test bench comprised of a variable injection circuit and high-resolution TDC, synchronized by a 1 GHz system clock, is used to measure the AFE timing resolution. The design is fabricated as a 32-channel prototype ASIC, and includes high-speed custom IO IPs.

Summary (500 words)

The intent of the project is to develop a next-generation AFE capable of approximately the same performance requirements as the recently designed ItkPix/CROC readout for the HL-LHC upgrade, but adding a timing requirement, and at the new CERN/HEP target node of 28 nm for increased digital capability. The BigRock prototype ASIC was submitted as mini@sic on the Feb 2022, 28 nm TSMC HPC+ IMEC run. It will be tested in the summer of 2022, with in-silicon results available for the conference presentation. It is comprised of 32 channels with two main modules:
• An AFE consisting of a preamplifier, comparator, and digital buffer
• An injection circuit and dual TDC with ˜ 5 ps resolution, recording the ToT leading and trailing edge time referenced to a 1 GHz synchronous system clock

A low-power TDC will be a follow-on development to complete the 4D front end. In this initial iteration, the channel TDC is intended only as an on-chip testbench for the AFE, avoiding timing uncertainties in the interface and test PCB. Therefore, the TDC in this prototype is essentially unconstrained in design parameters, excepting resolution. In addition, fast custom IO was developed for the system clock and internal test point signals:
• LVDS receiver
• CML driver

A preamplifier based on the prior art in [1] is the central element of the BigRock prototype project. Several current-mode CSA/TIA topologies were evaluated for the application, with this topology providing the most balanced performance metrics. The analog requirements are namely:
• analog current consumption of ˜4 uA
• noise < 100 e- RMS @ 50 fF detector capacitance
• ToT precision commensurate with timewalk correction
• hit timing requirement of ˜50 ps RMS resolution for 4D tracking
• performance met at a 0.15 fC threshold with 0.5 fC central charge injection

To maintain the integrity and simplicity of the current-mode path, a current comparator is implemented in place of the voltage comparator of previous designs. This is a straightforward cascoded current source design with a global threshold reference current. Pixel offsets are anticipated to be trimmed at a voltage reference point in each pixel preamplifier, with simulations indicating a requirement of 6 trim bits spanning 100 mV.

The TDC is described in [2]. It has a coarse register that counts up to 63 system clocks (1 ns), and a 128-stage delay line to divide the system clock. There are two TDCs per channel, recording each edge of the ToT signal.

Thus, the readout is a serial register for each ToT edge that contains (6 + 128) bits, representing the number of clocks plus the fractional clock period time from the last clock before the TDC counter is frozen. The injection circuit has 4-bits of programmability, and a variable injection reference voltage on the first stage to allow for fine tuning in the range 100's of electrons.

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