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A 65nm Dual Mode 1.25/7 GHz PLL with CML Line Driver for ALICE ITS3 and EIC Applications

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This paper presents a dual frequency PLL designed to support data transmission in next generation particle physics detectors. The PLL is designed in a 65nm CMOS process and operates in two frequency modes 1.25GHz in the lower frequency mode and 7GHz in the higher frequency mode. A PRBS generator is integrated with the PLL to enable testing and the design occupies 0.110um2 of silicon space. The design is intended for use in the ALICE ITS3 upgrade, and the Electron Ion Collider. Here we report test results on the supporting LVDS receiver and CML line driver, which have already been tested.

Summary (500 words)

INTRODUCTION

Demand for higher frequency data transmission circuits is increasing as modern scientific systems generate and process very high data volumes, and the availability of smaller technology nodes permits an increase in the speed of such circuits. A Phase Locked Loop (PLL) which generates a clock/carrier is an essential part of every communication system. In this paper we demonstrate a dual mode PLL with two speeds of operation. This allows it to support existing data read out systems (where the supporting infrastructure imposes a speed limit) and future systems (where the infrastructure can be designed to support higher rates). Such flexibility is important as the cost of chip developments increases. The design particularly targets the ALICE ITS3 upgrade and the Electron Ion Collider (EIC). For this reason, special schemes and design techniques are employed to make the design radiation tolerant and area efficient.

IMPLEMENTATION

The system consists of three main blocks: (i) LVDS Receiver (ii) PLL (iii) CML driver (Fig.1). The PLL consists of a Phase Frequency Detector (PFD), charge pump, loop filter, a voltage controlled oscillator (VCO) for each frequency mode and a frequency divider.

The PFD compares the phase of the input clock and the feedback clock from the frequency divider. A special topology is used for PFD to avoid dead zones, thus improving the PLL jitter. The charge pump and loop filter use the PFD output to generate a control voltage for the VCO. The VCO is based on cross coupled delay cells, which allow high frequency operation with rail to rail signal swing. The gain of each VCO is selected such that the same loop filter can be used for both frequency modes. This allows a dramatic reduction in circuit area given the degree to which the loop filter dominates the size. The output of VCO is fed back to frequency divider, which features dynamic flip flops to support high frequency operation and employs an SEU immune architecture. Divider stages are also shared between both the frequency modes to reduce overall area. This increases the complexity of the circuit but gives the advantage of lower power and area.

For test purposes, the output of the PLL is transmitted off-chip via a CML driver. There is a parallel path where the output of the PLL passes through a PRBS generator to allow Bit Error Rate (BER) testing of the complete link.

RESULTS AND CURRENT STATUS

The supporting LVDS receiver and CML line driver were already fabricated as part of the CERN Experimental Physics R&D Programme (EP R&D WP1.2) (Fig.2) and have been shown to be functional on silicon up to 700MHz (Fig.3 and Fig.4). This is limited by the available test system. To extend the scope of testing a new

test system is in development which will permit testing up to multi-GHz rates, and BER measurement using a PRBS. These results will also be reported.
Design of the full chip including these blocks, the PLL and the PRBS generator is complete, and will be submitted this summer.

Primary authors: MATHEW, Soniya; SEDGWICK, Iain; GUERRINI, Nicola; HODGES, Alexander; GONELLA, Laura; BORRI, Marcello; HELSBY, William; HILL, Andrew; GLOVER, James

Presenters: MATHEW, Soniya; SEDGWICK, Iain

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