A 64-channel waveform sampling ASIC for SIPM in space-born applications

Silvia Tedesco, Andrea Di Salvo, Angelo Rivetti, Mario Bertaina

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Abstract

The implementation of a 64-channel ASIC for the readout of Silicon Photomultipliers in space experiments is described. Each channel embeds 256 memory cells which sample the input information at 200 MS/s. A single cell includes a sampling capacitor, a single-slope analog-to-digital converter and a digital control logic. The digitization is carried out only if a trigger signal validates the time window thus saving power. Moreover, the cells can can be digitized in parallel to speed up the conversion phase. The ASIC is designed in a 65-nm CMOS technology and the target power consumption is 5mW/channel.

1 Summary

Silicon Photomultipliers (SiPMs) are being considered for future space missions to detect the Cherenkov light produced by the interaction of Ultra-High Energy Cosmic Rays (UHECRs) with the Earth atmosphere. In these applications, it is of interest to capture snapshots of few hundreds of nanoseconds around a given trigger, while low power consumption is at a premium. Architectures that combine fast waveform sampling with low power and low speed digitizers are thus preferred to topologies employing fast but more power-hungry ADCs immediately after the input amplifier. Hence, a 64-channels ASIC is being developed that includes a 256-cell analog memory in each channel which stores the input information at 200 MS/s. When the sampling is enabled, the storage capacitor is connected between the preamplifier output and a reference value. If a trigger signal is received, the cells enter the digitization phase, otherwise they are overwritten. The 256 cell array can work as a single buffer or it can be segmented into a maximum of 8 slots with 32 cells each to allow multi-buffering operation. The digitization is carried out by a single-slope ADC embedded in each cell. This allows to digitize all the samples in parallel, reducing the dead time. The ADC resolution can be programmed between 7 and 12 bits. However, care must be paid to guarantee adequate uniformity among the 256 single-slope ADCs in the same channel. In the ADC, one input of the comparator is connected to the top plate of the storage capacitor while the second one is kept fixed at a threshold value. When a conversion is performed, the top plate of the storage capacitor is connected only to the gate of a MOS transistor and thus behaves as a floating node. A voltage ramp is applied to the bottom plate. Due to charge conservation, the same ramp is reproduced on the floating node.

When the voltage on this terminal reaches the threshold, the comparator flips, triggering the storage into local registers of the output word of a Gray counter which is distributed to all the ADCs. This scheme has the advantage that the ramp signal is common to all ADCs in one channel, thus granting uniformity of the slope and thus of the ADC gain. This is important because the ADC are used to digitize samples belonging to the same waveform, thus a gain non-uniformity in the ADCs can introduce severe nonlinearity. Furthermore, the comparator fires always at the same point and errors due to input common mode variations are hence avoided. Considering that the 256 sampling capacitors represent a large load for the ramp generator, the switching of the bottom plates precedes of 2 clock cycles the beginning of the ramp. The ASIC is being designed in 1.2 V, 65-nm CMOS technology. The target power consumption is 5 mW/ch. The ASIC will be submitted for fabrication in the second half of 2022. In the poster, the ASIC architecture and the main design solutions will be presented.