A high-resolution clock phase shifter circuitry for ALTIROC (supporting document)

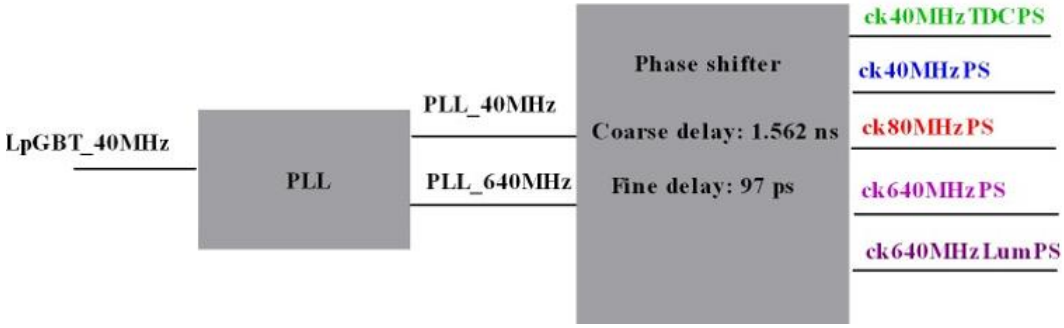

Figure. 1. Block diagram of clock generator in ALTIROC2. ALTIROC2 has an internal phase-locked loop (PLL), which produce 640 MHz and 40 MHz clock based on the reference 40 MHz clock from lpGBT. The phase shifter provides serval adjustable clocks including two 40 MHz, an 80 MHz, and two 640 MHz clock signals individually. The phase shifter was also used in ALTIROC1 and with the similar structure.

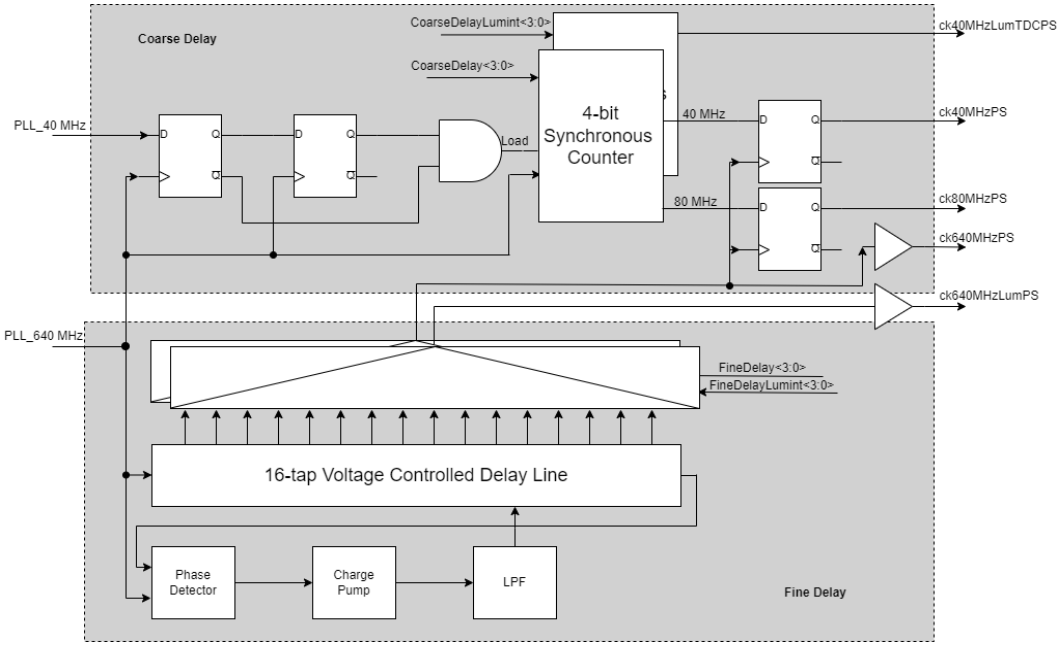

Figure 2. Block diagram of phase shifter for ALTIROC2. The tunable resolution of each clock is 1/640 MHz/16 = 97.7 ps. The phase shifter is a two-step architecture with a 25 ns coverage, consisting of a coarse-phase shifting with a 1.5625 ns step and a fine-phase shifting with a 97.7 ps step. The coarse delay is implemented by a counter producing 40 MHz, 80 MHz clocks from 640 MHz input clock. The fine delay is implemented with a delay-locked loop (DLL) operating at 640 MHz. The multiple clock signals are programmable independently and shared one DLL instance to save power consumption and area. The consistency of the delay of each delay cell in the delay line depends on a delay-locked loop (DLL), which called DLL based structure. A phase detector and a charge pump are adopted in the loop to obtain a stable locked status. A low-pass filter is used to stabilize the bias voltage coming from the charge pump in the

feedback loop. Two 16-to-1 multiplexers are used to output two separate adjustable fine-phase 640 MHz clocks. The combination of the coarse-phase shifter and the fine-phase shifter on the top uses the fine phases to resample the coarse phases to cover 25 ns tunable range.

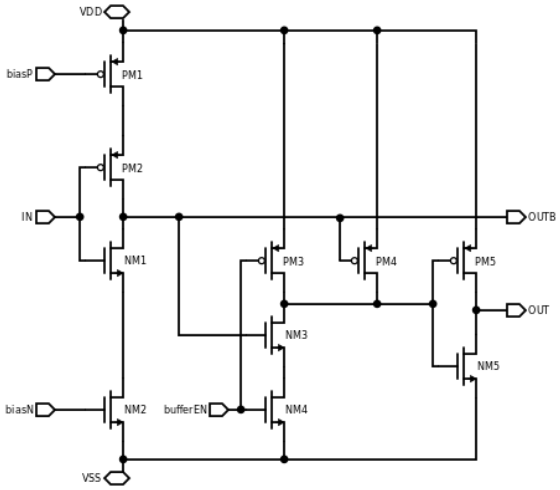

Figure 3. Schematic of a half delay cell. The delay cell consists of two cascaded current starved inverters to improve the clock signal duty cycle jitter. The starved inverter makes the delay of each delay cell adjustable along with the bias voltage. A brunch output is controlled by a NAN gate, which is the output buffer of each tap, and the dummies for the odd half delay cell in delay

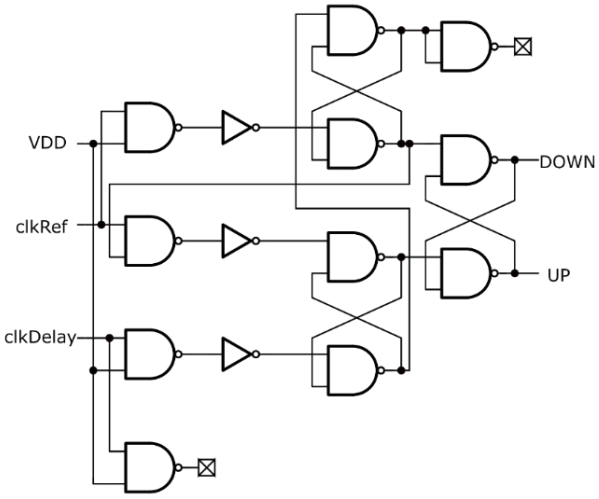

Figure 4. Schematic of the phase detector. The phase detector is used to compare the phase difference between the input and the output of the voltage-controlled delay line (VCDL). If the phase difference is small sufficiently, the loop locks in a stable state. The output pulse of the phase detector is to control the switches of the charge pump, which controls the bias voltage of the VCDL.

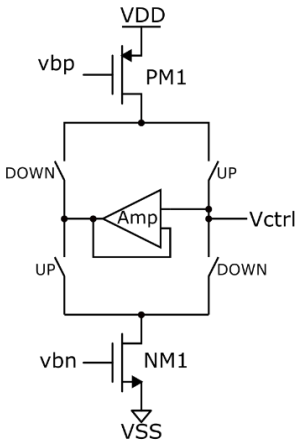

Figure 5. Schematic of the charge pump. The charge pump in Figure 5 has the current source coming from the PM1 transistor, and the current sink flowing into the NM1 transistor. The switches consisting of the transferring gate with a PMOS and an NMOS, turn on or off the current path to adjust the bias voltage (Vtrl) of the delay line. The bias voltage reveals the frequency of the VCDL linearly. The switches are controlled by the signals from the phase detector.

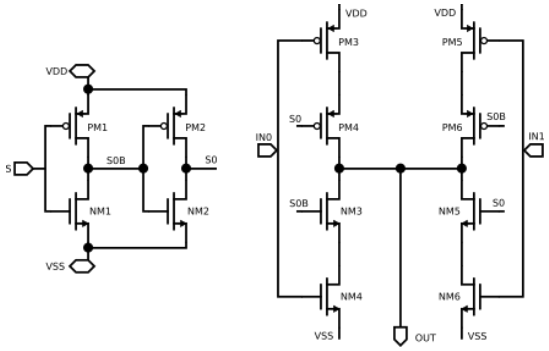

Figure 6. Schematic of a 2-to-1 multiplexer. The 16-to-1 multiplexer is implemented by a four-stage structure based on the 2-to-1 multiplexer. A 4-to-16 decoder is used to control the output of each multiplexer.

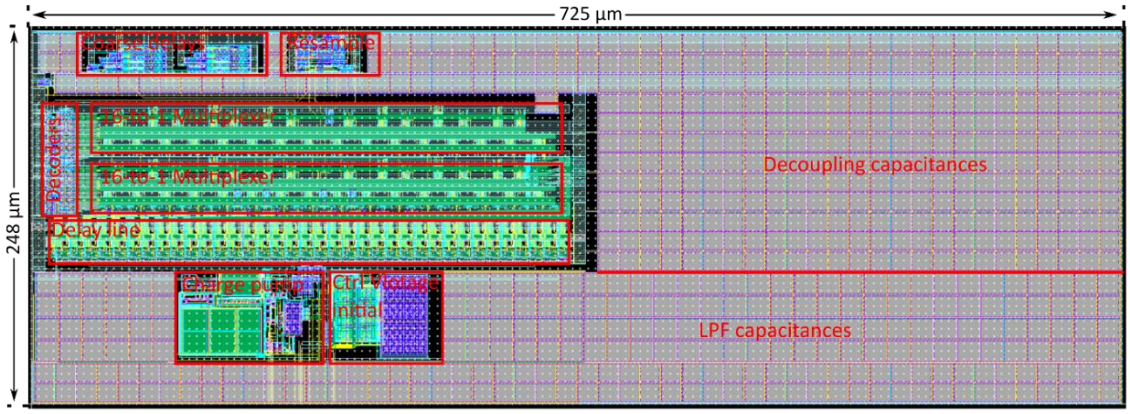

Figure 7. Screen shot of the phase shifter layout. The layout contains a shared delay line, two 16-to-1 multiplexers with decoders, two coarse delays, a charge pump, a phase detector, LPF, decoupling capacitors, and a bias voltage initial block. The area is 725 × 248 µm^2. The phase shifter work under 1.2 V

power supply voltage. The phase shifter is fabricated in a 130 nm CMOS process and tested as a separated module.

Figure 8. Diagram of test setup, and the picture of the test setup. The linearity and jitter performance were tested along with PLL. The internal PLL provides a 640 MHz, and a 40 MHz clock. The control bits are connected to the I2C module and controlled by the I2C bus. The phase shifter was tested by a high sampling rate electrical oscilloscope.

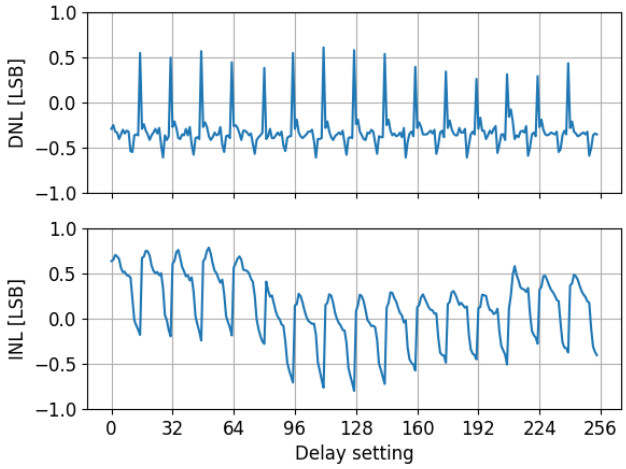

Figure 9. Test linearity of the phase shifter. The linearity of the clock phase shifter of the 40 MHz clock was measured. The DNL and INL are ±0.6 LSB and ±0.75 LSB, respectively.

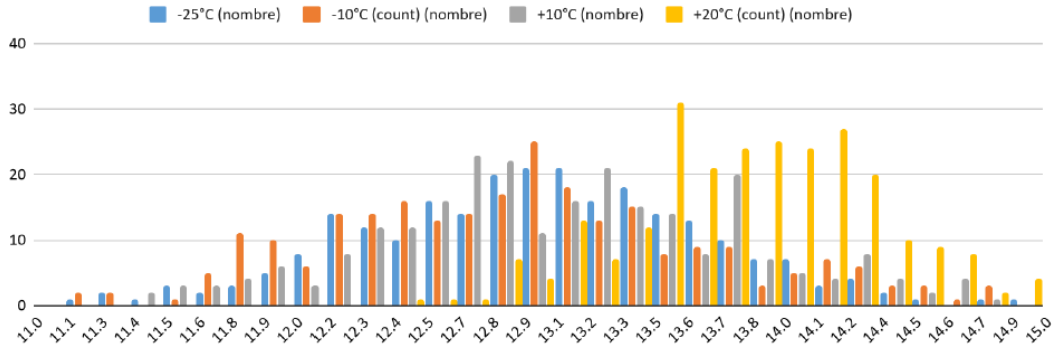

Figure 10. Jitter performance of the phase shifter. The jitter performance was tested with PLL. The accumulated standard deviation is 14 ps. The power consumption of the phase shifter module is 1.3 mW.

The TID test will be carried out along with ALTIROC in the future. The TID test results are to be reported in the workshop.