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A high-resolution clock phase shifter circuitry for ALTIROC

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A high-resolution clock phase shifter is implemented to adjust the phase of multiple clocks of 40 MHz, 80 MHz, and 640 MHz in the ALTIROC chip. The phase shifter is a two-step architecture, consisting of a coarse-phase shifting and a fine-phase shifting with a 97.7 ps step. The fine delay is a DLL-based structure operating at 640 MHz. The clocks are programmable independently and share one DLL to save power and area. The phase shifter is fabricated in a 130 nm CMOS process. The DNL and INL are ±0.6 LSB and ±0.75 LSB, respectively. The power consumption is 1.3 mW.

Summary (500 words)

The phase shifter is used for serval clock phases adjustment in ALTIROC, which is one of the readout ASICs for the High-Luminosity phase of LHC. The requirements of the phase shifter in ALTIROC are adjustable phases for multiple frequencies, 40 MHz, 80 MHz, 640 MHz, and the accuracy of 100 ps (period of 40 MHz dived by 256) with a full clock period coverage. To achieve the high accuracy of tunable phases in an efficient way while optimizing the power consumption and area, a two-step structure is adapted with a coarse-phase shifter and a fine-phase shifter. The full clock period phase adjustment is achieved by combing the coarse phase shifter and the fine phase shifter.

To cope with the 640 MHz clock coming from the internal PLL in ALTIROC, a configurable 4-bit counter is utilized to produce the dividing clocks of 80 MHz and 40 MHz. In the meantime, the configuration logic in the counter can adjust the dividing clocks with a step of 1.5625 ns, which implements the coarse phase shifting operations at both 80 MHz and 40 MHz clocks. The step of the coarse phase shifting is a period of 640 MHz clock. The function of the fine-phase shifting is further dividing the period of 640 MHz clock by 16. A delay line composed of 16 identical delay cells is interpolated in the period of 640 MHz. The output of each delay cell is the lowest significant bit (LSB) of the shifting phases.

The delay cell consists of two cascaded current starved inverters to improve the clock signal duty cycle jitter. The starved inverter makes the delay adjustable along with the bias voltage. The consistency of the delay of each delay cell in the delay line depends on a delay-locked loop (DLL). A phase detector and a charge pump are adopted in the loop to obtain a stable locked status. A phase detector is used to compare the phase difference between the input and the output of the voltage-controlled delay line (VCDL). The output pulse of the phase detector is to control the switches of the charge pump, which controls the bias voltage of the VCDL. A low-pass filter is used to stabilize the bias voltage coming from the charge pump in the feedback loop. The bias voltage reveals the frequency of the VCDL linearly. If the phase difference is small sufficiently, the loop locks in a stable state.

The coarse phase will be resampled by the fine phase, which obtains a 25 ns coverage. The combination on the top uses the fine phases to resample the coarse phases. An auxiliary circuit is proposed to avoid metastability during the resampling operation. The phase shifter is designed in a 130 nm CMOS technology and occupies 725 × 248 μm2.

The linearity and jitter performance was tested. The DNL and INL are ±0.6 LSB and ±0.75 LSB, respectively. The accumulated standard deviation of jitter is 14 ps. The power consumption of the phase shifter module is 1.3 mW.

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