Supporting document

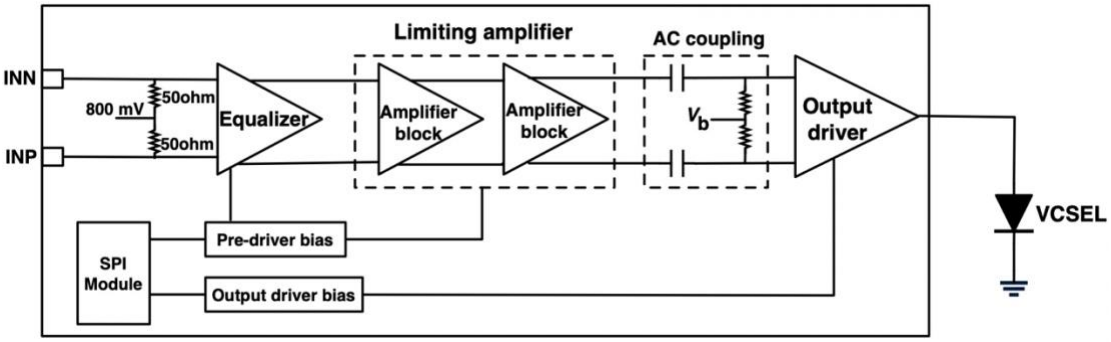

Figure 1 Block diagram of VCSEL driver ASIC

The block diagram of the 14 Gbps VCSEL driving ASIC is shown in figure 1. It consists of an equalizer stage, a limiting amplifier stage and a novel output driver stage. The equalizer stage receives a pair of 14 Gbps differential signals. The limiting amplifier stage receives the signals from the equalizer stage, and further amplifies the differential signals with sufficient gain and bandwidth for the output driver stage. The output driver stage converts the amplified differential voltage signals from the limiting amplifier stage to single-ended high speed current signal, and drives the external VCSEL.

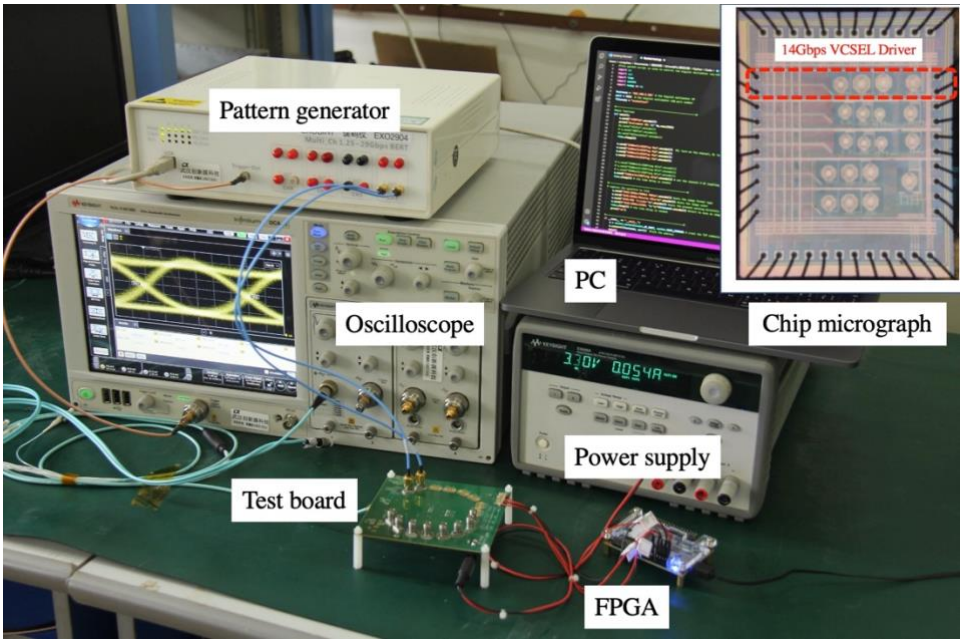

Figure 2 Test setup

During the test, a pattern generator (EXOSIHT EX02904) provides the 14 Gbps high-speed Pseudo-Random Binary Sequence (PRBS) signals. The final 14 Gbps eye diagrams are captured by the oscilloscope (Keysight DCA-X 86100D). The test setup is shown in figure 2.

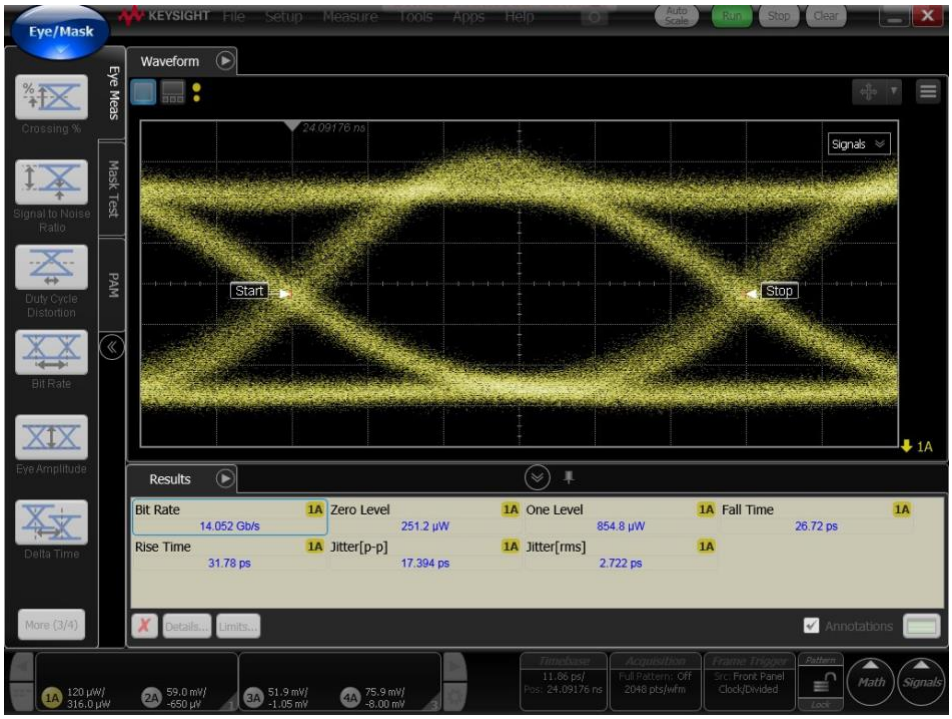

Figure 3 14 Gbps optical eye

Figure 3 shows 14 Gbps optical eye diagram with an optical amplitude of 603.6 μW. Wide-open eye is observed at 14 Gbps with a measured root mean square (RMS) jitter of 2.7 ps and a peak-to-peak jitter of 17.4 ps. The tested power consumption is 65.5 mW when working at the data rate of 14 Gbps.