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A 14 Gbps VCSEL Driving ASIC in 55 nm for NICA Multi-Purpose Detector Project

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This paper presents the design and the test results of a 14 Gbps VCSEL driving ASIC with a novel output driver structure fabricated in a 55 nm CMOS process. To increase the voltage headroom of the output driver stage and improve the bandwidth, a novel output driver structure using the on-chip AC coupling, the stacked current source and the double feedforward compensation technique is proposed. The test results show the wide-open 14 Gbps optical eye diagram with a measured RMS jitter of 2.7 ps and a peak-to-peak jitter of 17.4 ps, respectively.

Summary (500 words)

NICA (nuclotron-based ion collider facility) is a new accelerator complex designed at the joint institute for nuclear research (Dubna, Russia) to study properties of dense baryonic matter. It will provide variety of beam species ranged from protons and polarized deuterons to very massive gold ions. The multi-purpose detector (MPD) is one of three detectors in NICA and it has been designed to detect the charged hadrons, electrons and photons in heavy-ion collisions. The vertical cavity surface emitting laser (VCSEL) based array optical link is employed between the front-end and the back-end data transmission in the MPD readout electronics. The VCSEL driving ASIC is one of the key components in the VCSEL-based array optical link. This paper presents the design and the test results of a 14 Gbps VCSEL driving ASIC for NICA MPD project. It consists of an equalizer stage, a limiting amplifier stage and an output driver stage. The equalizer stage uses the CTLE structure to compensate the high frequency losses at the PCB traces, bonding wires and input pads. To meet both the gain/bandwidth requirements and the area restriction, the limiting amplifier stage adopts the inductor-shared peaking technology.

The threshold voltage of the VCSEL is around 1.6 V and some research indicates that the threshold voltage of the VCSEL may increase in high radiation environment. The output driver stage needs high power supply to provide sufficient voltage headroom to fit with the VCSEL threshold voltage. However, the MOS core voltage of the submicron CMOS process is quite low (CMOS 55 nm core voltage is 1.2 V), and the high voltage MOS transistors cannot be used in the high-speed design like the VCSEL output driver stage. This conflict brings the main difficulties to design the high-speed VCSEL driving ASIC. To solve this problem, a novel output driver stage is proposed with the combination of the on-chip AC coupling, the stacked current source and the double feedforward compensation structures to increase the voltage headroom and improve the bandwidth.

This ASIC has been integrated with the VCSEL array in a customized optical module for the optical test. Wide-open eye is observed at 14 Gbps with a measured RMS jitter of 2.7 ps and a peak-to-peak jitter of 17.4 ps. The tested power consumption is 65.5 mW when working at the data rate of 14 Gbps.

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