A radiation hard bandgap voltage reference for the ARCADIA project

G. Traversi[a,c], L. Gaioni[a,c], M. Manghisoni[a,c], M. Pezzoli [b,c], L. Ratti[b,c], V. Re[a,c]
on behalf of the ARCADIA collaboration

[a] University of Bergamo, Italy
[b] University of Pavia, Italy
[c] INFN Pavia, Italy

ABSTRACT

This work presents the design and characterization of a radiation hard bandgap reference circuit fabricated in a 110nm CMOS technology for the Main Demonstrator chip of the ARCADIA project. The design, based on a current-mode approach in order to be able to output a smaller than 1.2V reference voltage, employs diode-connected MOSFETs instead of BJTs to enhance the radiation hardness and a second amplifier to improve the current mirror of the output branch and therefore the line regulation of the circuit. This paper describes the features of the circuit and its measured results.

SUMMARY

A bandgap voltage reference is a block of paramount importance in both analog and mixed-signal circuits: it is used to provide a reference voltage, constant and independent, as much as possible, of process variations, supply voltage, and temperature. It combines an element that shows characteristics Proportional To the Absolute Temperature (PTAT) with another one that features Complementary To the Absolute Temperature (CTAT) characteristics using a circuit that is insensitive to variations on the supply voltage or to process parameters fluctuations. Conventional BGR architectures, also named voltage-mode bandgap, generate an output voltage of about 1.2V, which is close to the core supply voltage of the currently widespread CMOS technology, such as the 110nm one used in this work. However, several solutions employing a current-mode approach have been implemented allowing sub-1V operation.

This work will focus on the design of a current-mode bandgap reference that will be used in the ARCADIA (Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays) project, which aims at developing a sensor with fast charge collection, a scalable readout and low-power capabilities. Towards this goal, the collaboration has worked on a first main demonstrator: a low-power, high-density (25μm pitch) pixel matrix of CMOS monolithic sensors developed for both HEP (future colliders) and space applications. Both applications pose some additional requirements to the design of the circuit that have to be faced. The high fluences expected the future colliders advise against the use of bipolar transistors, due to their sensitivity to bulk damage. On the other hand, deep-submicron CMOS technologies, thanks to the reduced thickness of the gate oxide and with the addition of some layout techniques, have demonstrated to be resistant to hundreds of Mrad of TID and can be used to implement a radiation-tolerant bandgap voltage reference.

The circuit described in this work is based on enclosed-layout, diode-connected MOSFETs biased in weak inversion region, which, together with DTMOST devices, are the main devices that have been proven inherently radiation hard due to the absence of any thick oxide near the pn-junction. The design also includes two programmable resistors that allow to adjust the voltage-to-temperature slope and the absolute value of the reference voltage respectively.

The conference presentation will discuss the main design solutions and some relevant simulation results together with the results of the characterization activity.