Fast prototyping of Front End ASICS and validation of associated DAQ with a Cadence Protium platform.

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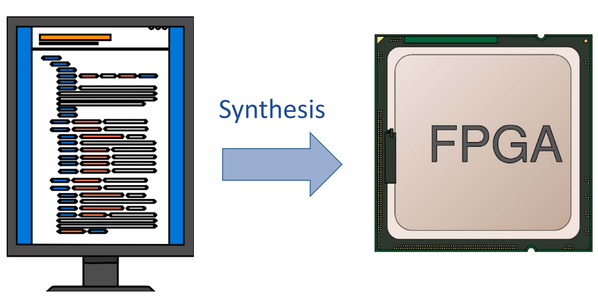
Abstract

ASICs designed for HEP embed always more digital components and require complex and critical verifications. Prototyping enables implementations of digital part of ASIC in programmable components such as FPGA. Interactions with external devices such as DAQ, micro-controller or other FPGA are then possible. Debugging of internal firmware or complex stimuli becomes easier and faster than time-consuming simulations.
Cadence PROTIUM is an FPGA based solution that allows ASIC designers to easily and automatically prototype the RTL code of their ASIC. At IPHC, it was used to do the functional validation of several ASICs and DAQ system.

ASICs Prototyping

Principle

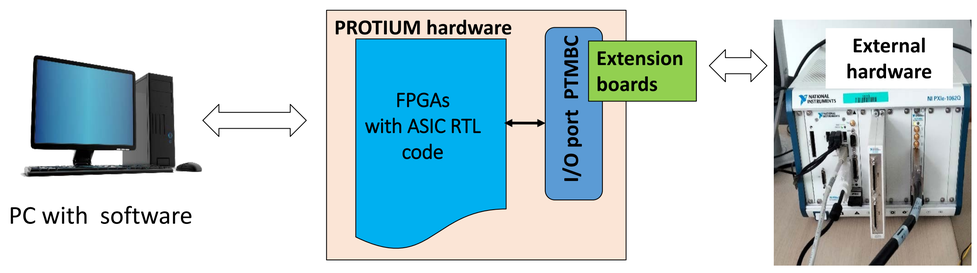
Map ASIC RTL code into FPGAs



Benefits of FPGA prototyping:
- Pre-silicon verification
- Firmware/Software verification
- Connect hardware
- Cheaper than multiple ASIC respin

What is Cadence PROTIUM platform?

PROTIUM = FPGAs board
+ dedicated Software (Cadence + Xilinx Vivado)
+ extension boards for hardware connections (RAM, I/O, FMC,…)



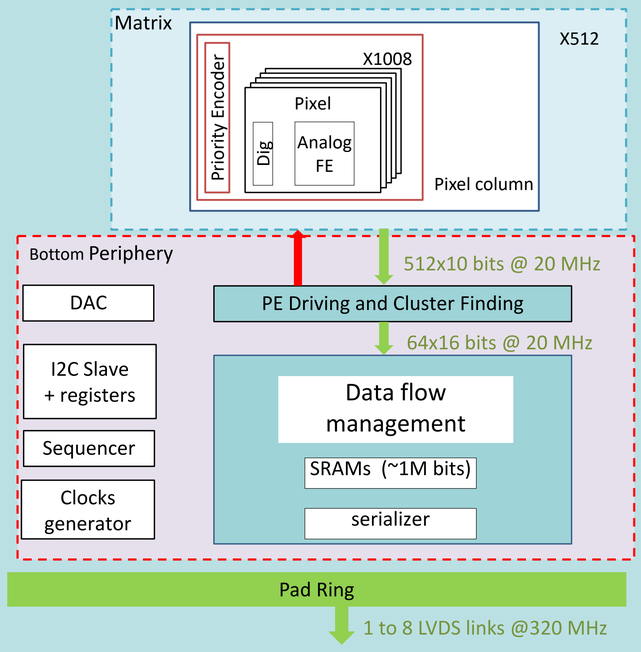
PROTIUM FPGAs = Xilinx Ultrascale VU440
(equivalent to 2 Virtex 7)

Why IN2P3 chose PROTIUM?

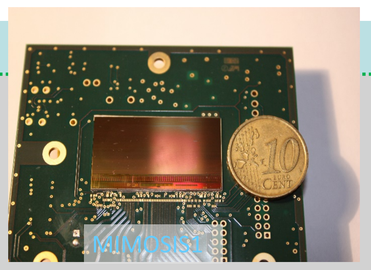
- PROTIUM keep the original ASIC RTL code
  => **no need to modify** the ASIC code to fit FPGAs architecture
- **Easy to use**
  => no need of special FPGA skills
- **Accelerates** the **DAQ** and slow control **development**
- **Black Box** flow:
  - **ASICs and IPs** (custom or Xilinx) connected **inside the same FPGAs**
  - **Allow system integration** (see F.Morel's poster)

Verification with PROTIUM of digital parts of MIMOSIS 1 & 2

MIMOSIS1 & 2 synoptic

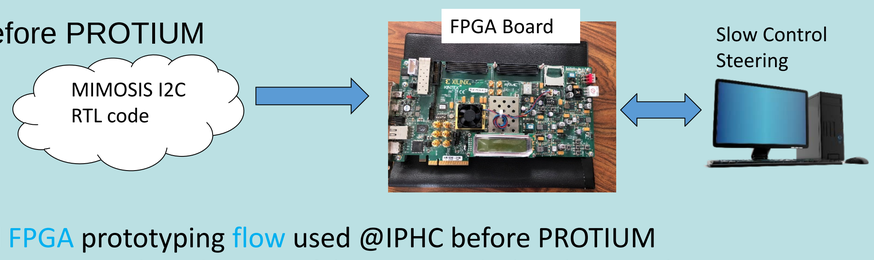


MIMOSIS 1 & 2
- Designed for the **CBM-MVD** in a **180 nm CIS** technology
- **Reticle size ASIC** (17x31 mm²), **0,5 million of pixels** (digital logic in each pixel)
- **MIMOSIS1** produced in **2020**
- **MIMOSIS2** Taped Out in **Sept 2022** with Clocks, reset and FSM **fully tripled** with CERN TMRG tool



Slow control validation for MIMOSIS chips

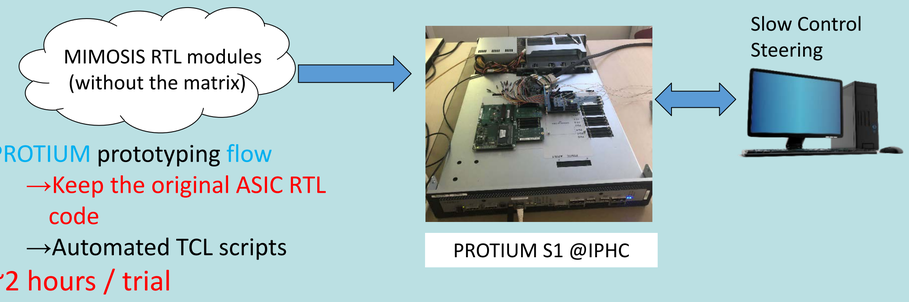
- Before PROTIUM



Classical FPGA prototyping flow used @IPHC before PROTIUM
Manual conversion and simplification of the I2C RTL code done by FPGA designer :
→Remove Triple Vote
→Remove clock gating

Highly man power consuming : 1 week / trial !

- With PROTIUM

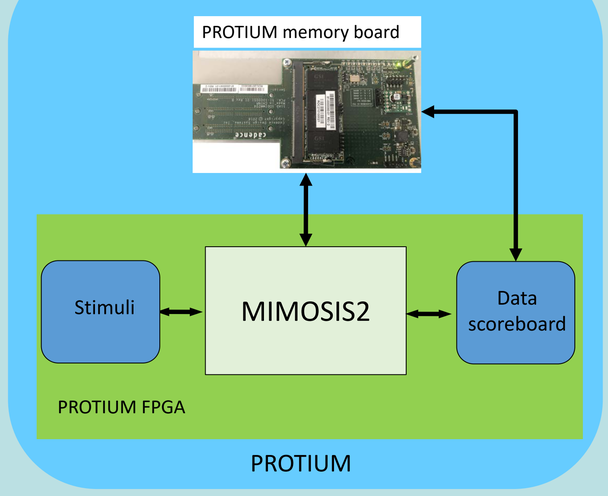


PROTIUM prototyping flow
→Keep the original ASIC RTL code
→Automated TCL scripts
~2 hours / trial

PROTIUM S1 @IPHC

A common platform for designers & test engineers

Data Flow verification for MIMOSIS 2



PROTIUM Memory board:
- **Store stimuli and results**
- **Emulates the matrix**
  (1 FPGA instead of 6 needed)

Data readout test :
- **Standard mode** (in development)
  ↳Replace pixel matrix with PROTIUM memory board
- **Test mode** (ASIC feature)
  ↳injection of stimuli into the bottom periphery via dedicated I2C registers.

Simulation vs Prototyping run time test

1300 I2C R/W access (all MIMOSIS1 registers)	UVM Testbench	PROTIUM + hardware I2C + DAQ software
Runtime needed	63 min	1,8s

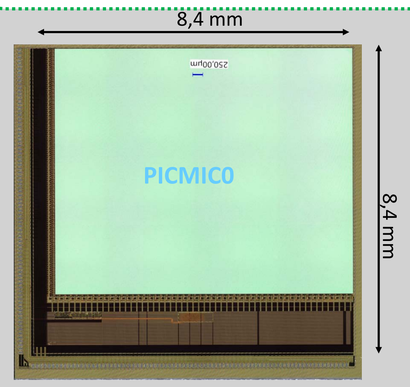
I2C update and debug for MIMOSIS2

Bug detected in the **I2C watchdog** during the test of MIMOSIS1
↳ correction and validation of the **new RTL** code in PROTIUM for MIMOSIS2
↳**same** PROTIUM **scripts** and **slow control steering** for MIMOSIS1 and MIMOSIS2

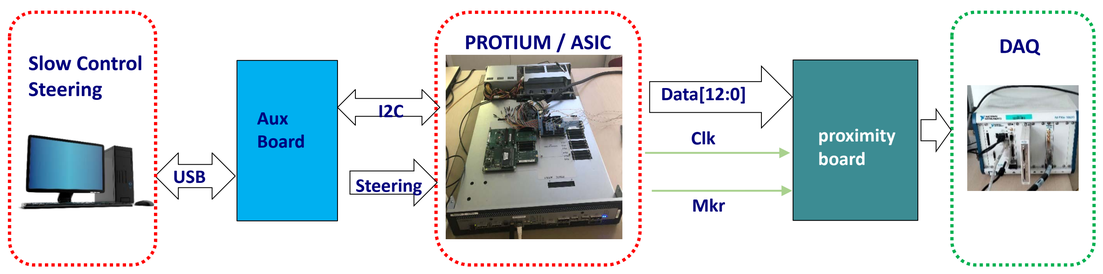
Validation of PICMIC0 system before Tape Out

PICMIC0 ASIC

- **IN2P3 collaboration** (IPHC & IP2I)
- Encodes **hits positions** from an Micro Plates Chamber Detector (**MCD**)
- **Each pixel** embedded an **I2C register** for hit emulation
- Produced in **Q2 2022** (180 nm CIS)



DAQ system chain for PICMIC0



Benefits of PROTIUM flow for this project :
- **Early development of DAQ and slow control**
- **ASIC functional verification with external hardware system**
  - I2C chain driven by an external **Arduino** (DAQ software and hardware extensive checks with 1 million R/W cycles in less than 3 hours)
  - Data readout tested with DAQ and data analysis software
- **Same software and hardware for ASIC validation and PROTIUM flow**

Benefits from PROTIUM usage on IPHC projects

- **ASIC Verification** improved before Tape Out
- **Early development** of DAQ and slow control systems
- **Common platform** between ASIC designers and test engineers
  ↘↘ man power cost, ↗↗ project closure
- **High capacity FPGAs** available
  - Reticle size MAPS with full pixel matrix.
  - Embedded software such as RISCV dev.
  - IA development such as smart trigger

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