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Fast prototyping of Front End ASICS and validation of associated DAQ with a Cadence Protium platform.

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ASICs designed for HEP embed always more digital components and require complex and critical verifications. Prototyping enables implementations of digital part of ASIC in programmable components such as FPGA. Interactions with external devices such as DAQ, micro-controller or other FPGA are then possible. Debugging of internal firmware or complex stimuli becomes easier and faster than time-consuming simulations.
Cadence Protium is an FPGA based solution that allows ASIC designers to easily and automatically prototype the RTL code of their ASIC. This platform and its use for the validation of several ASIC DAQs and slow-controls developed at IPHC will be presented.

Summary (500 words)

MIMOSIS-1, the first full size pixel sensor prototype developed for the CBM-MVD (FAIR/GSI), incorporates over 40 million of digital gates. It integrates custom digital cells in every pixels of the matrix (˜1/2 million of pixels), sparse data read-out and elastic buffer to deal with a large and fluctuating data flow (up to 2.4 Gbits/s). For this kind of sensor, the need of a smart and robust verifications before tape out is crucial.
Simulations allow designers to have a fine granularity in verification of frontend and backend netlist. Designers can probe and check every nets and registers of their design. Constrained random stimuli (as in UVM testbenches) improve the verification procedures. However, it needs high number of stimuli to achieve a good functional coverage score. Furthermore, the more the size of the design increase, the more the simulation needs resources (CPU time, memory, license tokens). Checking the interactions between the ASIC under test and external hardware devices, especially DAQ systems, could be tricky, mostly due to a lack of a fine simulation model of the later.
Prototyping offers a complementary solution. It implements a functional model of the ASIC in programmable devices. This prototype is simply plugged to the DAQ and tested. The verification is easier, the time needed to test huge number and complex test scenari is reduced compared to simulation.
MIMOSIS-1 slow-control integrates an I2C chain. Radiation hardness tolerance requires for this module a triplication generated with CERN TMRG tools. For functional verification purpose, this I2C chain has been prototyped in a generic FPGA board. Due to specific hardware architecture limitations, some modifications of the RTL code were done (removal of triplication and clock gating). This manual adaptation was time-consuming, could have introduced bias (adding or correcting bugs) and need to be done every time the ASIC code changes.
Cadence Protium is a prototyping solution based on hardware environment (mainly a Xilinx Ultrascale VU440 FPGA) with dedicated software. Contrary to generic FPGA platform, ASIC designers don't need neither to adapt their RTL code neither to FPGA knowhow. All the steps are scripted in TCL language and can be replayed in case of modification of the ASIC source code.
The slow-control and the data readout of MIMOSIS-1 were successfully implemented and tested in a Protium connected to a dedicated slow-control monitor. Compare to the FPGA approach, the prototyping is much faster (0.5 day vs ˜1 week/try). MIMOSIS-2, an evolution of Mimosis1, will use the same slow-control. As the code in the ASIC and in the prototype is the same (ex: triplication is kept), Protium allows to validate by hardware new features and bug corrections.

Another ASIC, PICMIC, dedicated to microchannel plates detector and developed in collaboration with IP2I laboratory, was also fully implemented in Protium in order to develop the DAQ and slow-control monitor. This time, it allowed verifying the ASIC data readout with the whole DAQ and perform hardware functional tests, weeks before the chip actually came back from foundry.

Primary author: Mr BERTOLONE, Grégory (Université de Strasbourg,CNRS,IPHC)

Co-authors: Mr COLLEDANI, Claude Pierre (Université de Strasbourg,CNRS,IPHC); CLAUS, Gilles Lucien (Centre National de la Recherche Scientifique (FR)); Mr SCHOTT, Hugo (Université de Strasbourg,CNRS,IPHC); JAASKELAINEN, Kimmo Kalevi; Mr SPECHT, Matthieu (Université de Strasbourg,CNRS,IPHC); PHAM, Thanh Hung (Université de Strasbourg,CNRS,IPHC); Dr ZHAO, Yue (Université de Strasbourg,CNRS,IPHC)

Presenter: Mr BERTOLONE, Grégory (Université de Strasbourg,CNRS,IPHC)

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